linPOL48V_V2

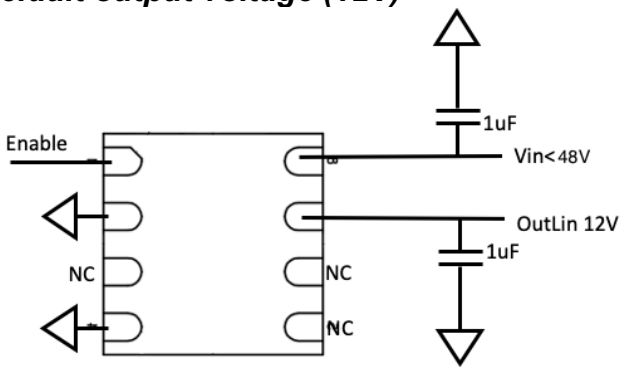
48V Radiation Tolerant Linear Regulator

Features
- Input voltage up to 48V
- One tunable output voltage, with default value 12V, maximum 13V
- Continuous 200mA load capability
- Input Under-voltage lockup
- Enable Input

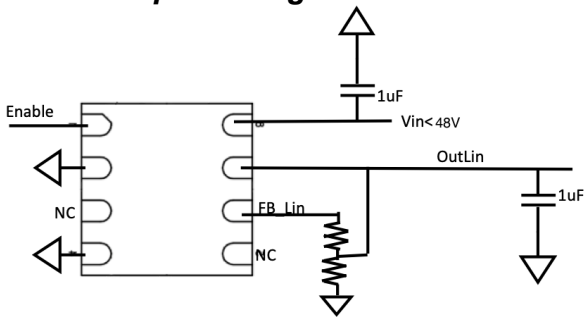
Applications
Point of Load in distributed power systems where radiation tolerance is required. This ASIC is developed to provide an efficient solution for the distribution of power in High Energy Physics experiments and for space applications. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the controller capable of continuous operation up to very high radiation limit (50Mrad and 4e14 n/cm2 and 2.23e14 p/cm2(30MeV proton beam).

Description
linPOL48V is a 48V rad-hard linear regulator. The default output voltages is 12V with maximum output current of 200mA.

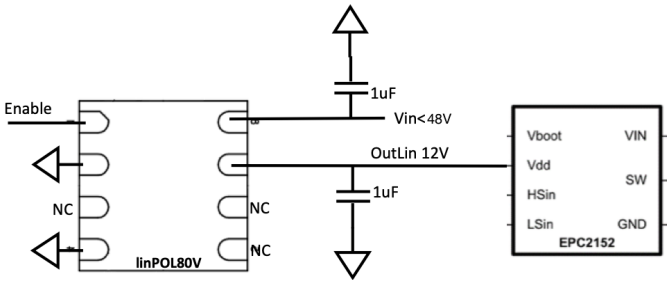
Typical application with default output voltage (12V)



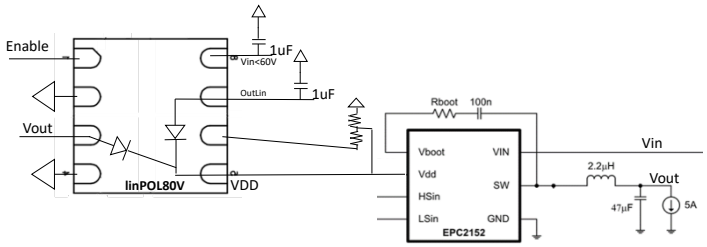
Typical application with modified output voltages



Typical application with EPC2152



Typical application with EPC2152, and Vout DCDC=12V

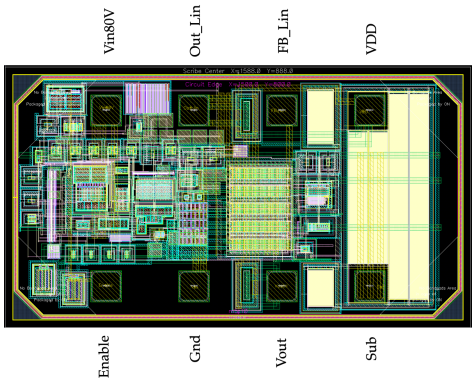


NB: The diodes depicted are internal in LinPOL48V

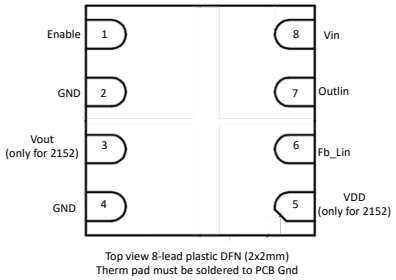
Absolute Maximum Ratings

Input Voltage Vin……..……...…-0.3V to +48.0V
Enable ……..……...…-0.3V to +3.6V
Lin Reg feedback, FB_Lin……..……...…-0.3V to +3.6V
Linear reg. Output voltage, OutLin……..……-0.3V to +48.0V
DCDC Vout input, Vout……..……...…-0.3V to +48.0V
Output for VddEPC2152, Vdd……..……...…-0.3V to +48.0V

Bare die configuration



Pin Configuration



Top view 8-lead plastic DFN (2x2mm)
Therm pad must be soldered to PCB Gnd

Pin Function

Enable (Pin 1): Enable pin for the voltage regulator. It is active High. A voltage above 480mV is needed to enable the linear regulator. A voltage below 300mV is needed to disable the linear regulator. An internal pull-down resistor of 100KOhm is connected to ground.

Gnd (Pin 2,4): Ground of the ASIC. It must be connected to the PCB ground plane.

Vout (Pin 3) and VDD (Pin 5): these have to be used only with EPC2152 when the Vout of the DCDC converter is 12V.
In order to achieve higher efficiency for the full converter (EPC2152+LinPOL48V), the VDD of EPC2152 is supplied at the beginning from the linear regulator and after from the output of the DCDC converter since its conversion efficiency is much higher (above 90%).
Please refer to the "*Typical application with EPC2152, and Vout DCDC=12V"* schematic. VDD is connected to EPC2152 Vdd and Vout is connected to the Vout of the DCDC converter.
Inside LinPOL48V two diodes are placed between Vout and VDD pin and OutLin and VDD. When Vout is higher than OutLin, VDD is supplied from Vout. Vdd will be regulated at 11V from the linear regulator placing a resistance of 18KOhm between VDD and FB_lin and 2.2KOhm between FB_lin and GND. When Vout is higher than 11.7V (11V+Vfwd diode), the current to VDD will be provided by Vout.

Fb_Lin (Pin 6): Feedback point of the linear regulator. Adding a voltage divider between OutLin, Fb_Lin and GND it is possible to tune the OutLin output voltage. Internally the resistances used are 200KOhm between OutLin and Fb_Lin, 22KOhm between Fb_Lin and GND. Resistor with values below $1/10^{th}$ of the previously mentioned resistances have to be used to override the internal voltage divider. In steady state the linear regulator's amplifier will force this node to be 1.2V (equal to the Bandgap node). Please refer to the typical application scheme for different output voltage. It has to be left floating if the customer wants to use the 12V output voltage.

OutLin (Pin 7): Output voltage of the linear regulator, able to provide 200mA with a default value of 12V. Between this pin and ground a capacitor of 1uF has to be placed for stability purpose.

Vin (Pin 8): Input Voltage for the Linear regulator. It is recommended to add a capacitor of 1uF between Vin and Gnd.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - Vin	-	48	V
Output voltage - OutLin	1.2	13	V
Enable Voltage - Enable	0	3.3	
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	ºC

Block Diagram

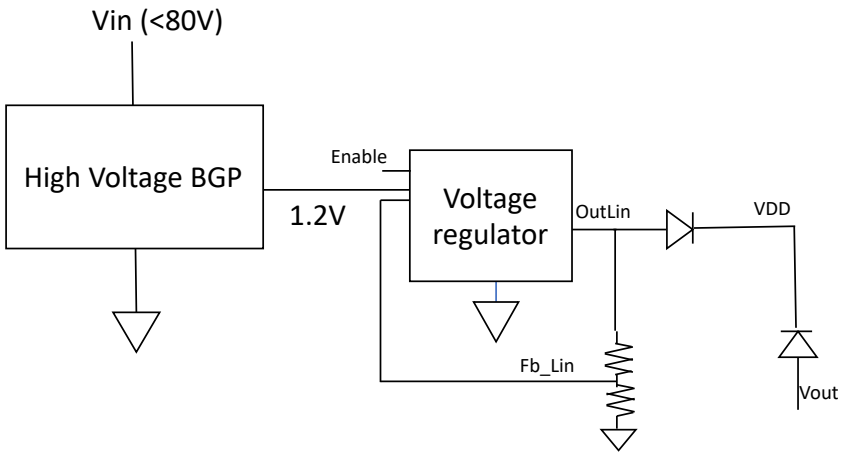
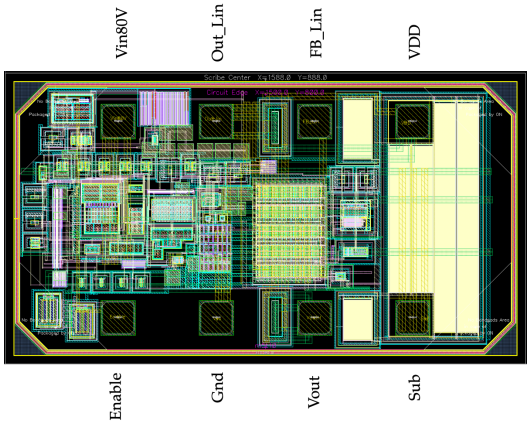


Figure 1: Block diagram of the linPOL48V ASIC.

Bare die description

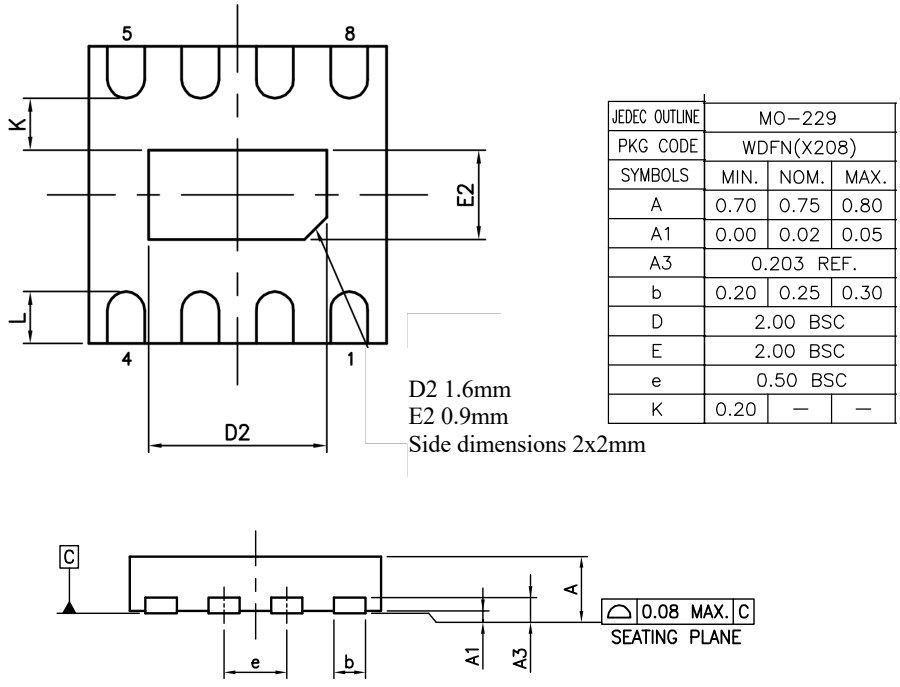
linPOL48V is also available as naked chip, Chip dimension 1.5mmx0.8mm, pad dimension 90umx90um, pitch: horizontal 300um, vertical 600um. The coordinates of the pads, having 0,0 in bottom left corner, are presented in the following table



Pin	X (um)	Y (um)
Enable	344	140.25
Vin48V	344	740.25
Out_lin	644	740.25
FB_Lin	944	740.25
VDD	1244	740.25
Sub	1244	140.25
VoutH	944	140.25
Vss	644	140.25

Package description

linPOL48V is packaged in a plastic Dual Flat No-Lead (DFN) package 2.0x2.0x0.9mm in size, with 8 pads and with an exposed pad to be soldered to the PCB for better thermal properties. The suggested PCB layout for the integration of linPOL48V is shown in the following figure. The dimension of the signal pads is 0.25x0.5mm and the one of the central exposed thermal pad is 1.6mmx0.9mm. All distances are referred to the center of the signal or exposed thermal pads.



JEDEC OUTLINE	MO-229		
PKG CODE	WDFN(X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.00 BSC		
E	2.00 BSC		
e	0.50 BSC		
K	0.20	—	—

Figure 3: Suggested PCB layout for the integration of the linPOL48V DFN8 package.

Revision history

Revision	Date	Description
1.0	2/9/2020	First release of the document.