linPOL12V

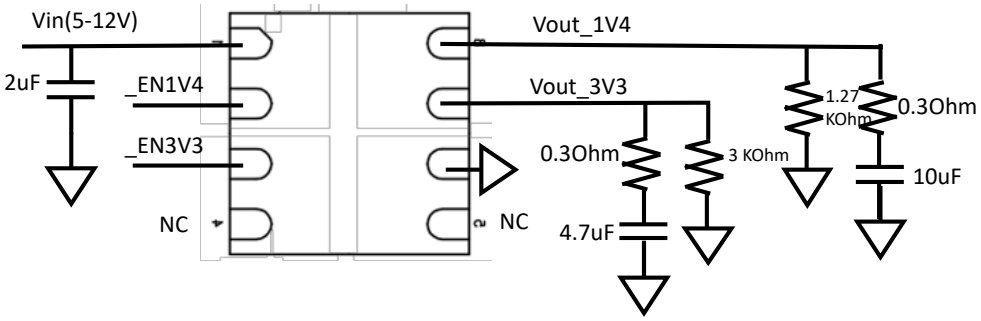
Dual Radiation Tolerant Linear Regulator

Features
- Input voltage range 5 to 12V
- Two tunable output voltages, with default values 3.3V and 1.4V
- Continuous 25mA load capability for 3.3V output and Continuous 80mA load capability for 1.4V
- Input Under-voltage lockup
- Enable Input
- TO BE TESTED FROM EXPERIMENT USERS
  ATLAS and CMS are running radiation testing, results will be available soon

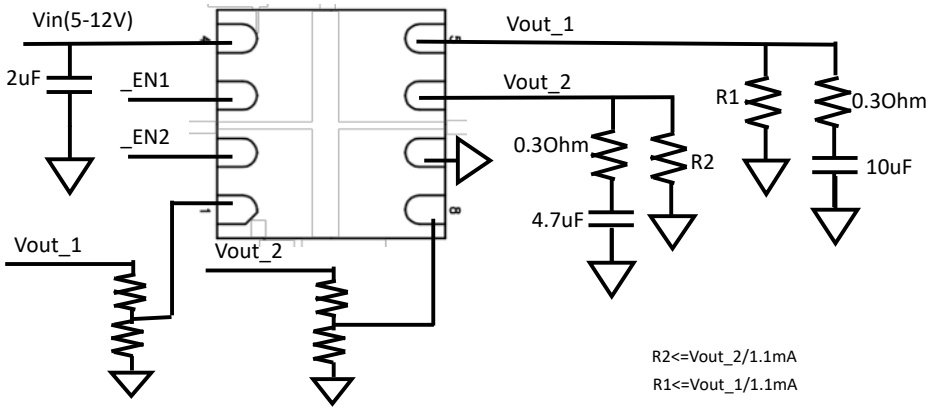
Applications
Point of Load in distributed power systems where radiation tolerance is required.

Description
linPOL12V is a dual output, single input rad-hard linear regulator. The two default output voltages are 1.4V and 3.3V with respectively maximum output current of 80mA and 25mA.

Typical application with default output voltages (3.3V and 1.4V)



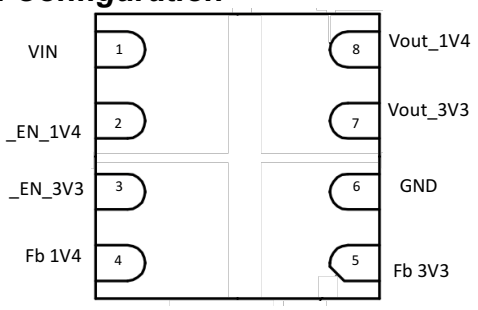
Typical application with modified output voltages



Absolute Maximum Ratings

Input Voltage Vin……..……...…-0.3V to +12.0V
Enable pins (_En1V4 and _En3V3)…….…...….-0.3V to +3.6V
Vout pins (_En1V4 and _En3V3)…….…….....….-0.3V to +3.6V
Feedback pins (Fb_1V4 and Fb_3V3) ….....….-0.3V to +3.6V

Pin Configuration



Top view 8-lead plastic DFN (2x2mm)
Therm pad must be soldered to PCB Gnd

Pin Function

Vout_1V4 (Pin 8): Output voltage of the first linear regulator, able to provide 80mA with a default value of 1.4V. Between this pin and ground a series of a resistor of 300mOhm and a capacitor of 10uF has to be placed for stability purpose. A resistance towards ground must be placed to avoid a TID-induced peak at 1-2Mrad. The value of the resistance must be set to have at least 1.1mA always flowing in the regulator. Therefore R<=Vout/1.1mA which is 1.27KOhm if Vout is 1.4V (default value if Fb_1V4 is left floating).

Vout_3V3 (Pin 7): Output voltage of the first linear regulator, able to provide 25mA with a default value of 3.3V. Between this pin and ground a series of a resistor of 300mOhm and a capacitor of 4.7uF has to be placed for stability purpose. A resistance towards ground must be placed to avoid a TID-induced peak at 1-2Mrad. The value of the resistance must be set to have at least 1.1mA always flowing in the regulator. Therefore R<=Vout/1.1mA which is 3KOhm if Vout is 3.3V (default value if Fb_3V3 is left floating).

Gnd (Pin6): Ground of the ASIC. It must be connected to the PCB ground plane.

Fb_3V3 (Pin 5): Feedback point of the 3.3V linear regulator. Adding a voltage divider between Vout_3V3, Fb_3V3 and GND it is possible to tune the Vout_3V3 output voltage. Resistor with values below 10KOhm has to be used to override the internal voltage divider (500KOhm). In steady state the linear regulator's amplifier will force this node to be 600mV (equal to the Bandgap node). Please refer to the typical application scheme for different output voltage. It has to be left floating if the customer wants to use the 3.3V output voltage.

Fb_1V4 (Pin 4): Feedback point of the 1.4V linear regulator. Adding a voltage divider between Vout_1V4, Fb_1V4 and GND it is possible to tune the Vout_1V4 output voltage. Resistor with values below 10KOhm has to be used to override the internal voltage divider (500KOhm). In steady state the linear regulator's amplifier will force this node to be 600mV (equal to the Bandgap node). Please refer to the typical application scheme for different output voltage. It has to be left floating if the customer wants to use the 1.4V output voltage.

_En_3V3 (Pin 3): Enable pin for the 3.3V voltage regulator. It is active Low. A voltage above 600mV is needed to disable the linear regulator. An internal pull-down resistor of 100KOhm is connected to ground.

_En_1V4 (Pin 2): Enable pin for the 1.4V voltage regulator. It is active Low. A voltage above 600mV is needed to disable the linear regulator. An internal pull-down resistor of 100KOhm is connected to ground.

Vin (Pin 1): Input Voltage for the Dual Linear regulator. It is recommended to add a capacitor of 2uF between Vin and Gnd

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - Vin	5	11	V
Output voltage – Vout_1V4 Vout_3V3	0.9	3.3	V
Enable Voltage - _En_1V4 _En_3V3	0	3.3	
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	°C

Block Diagram

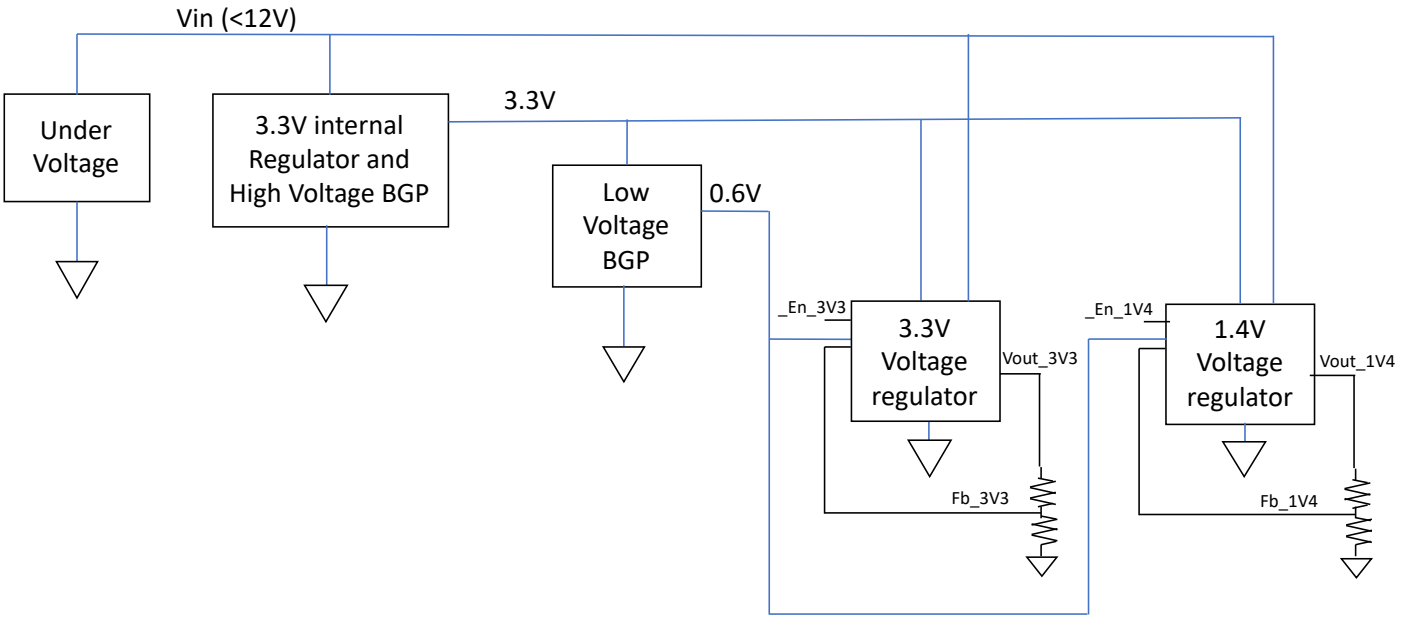


Figure 1: Block diagram of the linPOL12V ASIC.

Operation

linPOL12V is a dual linear regulator designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace.

Output voltage selection
The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout* and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage (BGP). This has been measured on previous integration. The average value is 600mV.

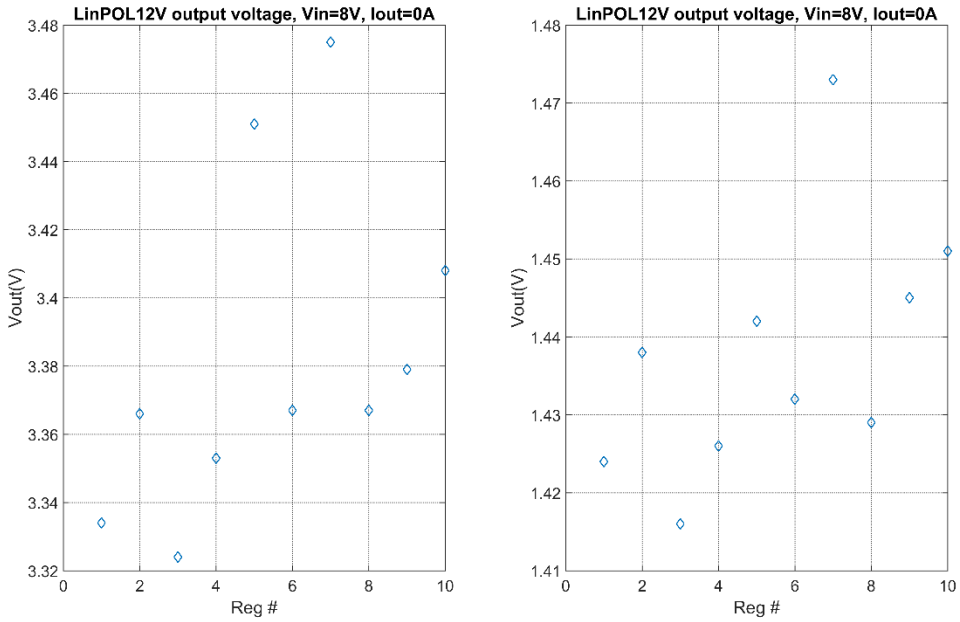
Embedded linear regulators
While it can operate from a supply voltage of up to 12V, the control electronics in linPOL12V requires powering at 3.3V. A linear regulator is embedded to provide appropriate voltage to reference voltage generator and the two output linear regulators.

Under-Voltage lockout
The embedded linear regulators need a sufficient level of over-voltage to provide stable 3.3V voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above about 4.8V (on rising Vin). This comparator has a hysteresis and linPOL12V is disabled again when, for falling Vin, the input voltage drops below about 4.5V.

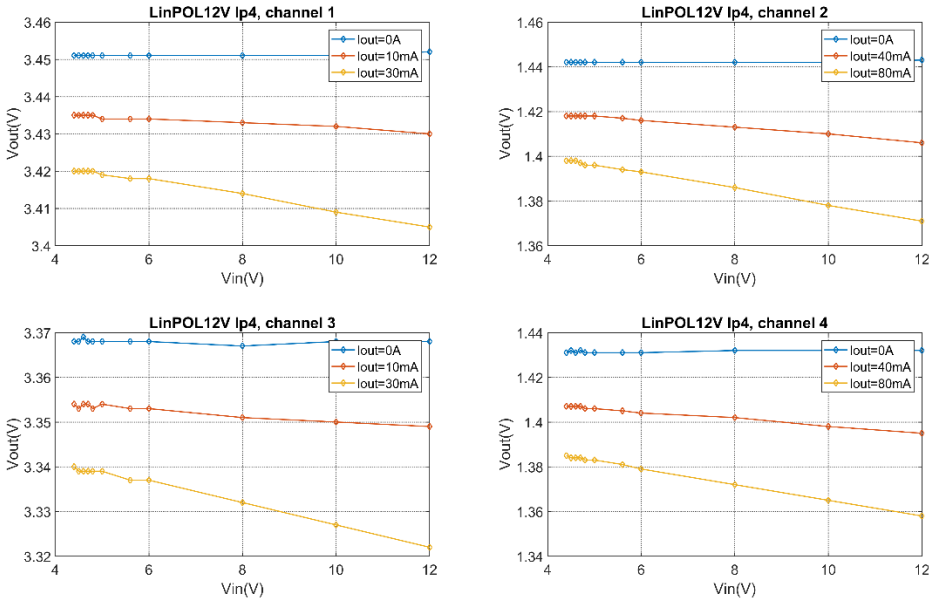
Enabling linPOL12V
The circuit is enabled by default thanks to the internal pull-down resistors on _En* nodes. It will start when a sufficient Vin is applied to its input. LinPOL can be disabled applying on the enable pins (_En*) a voltage higher than 600mV.

Test results

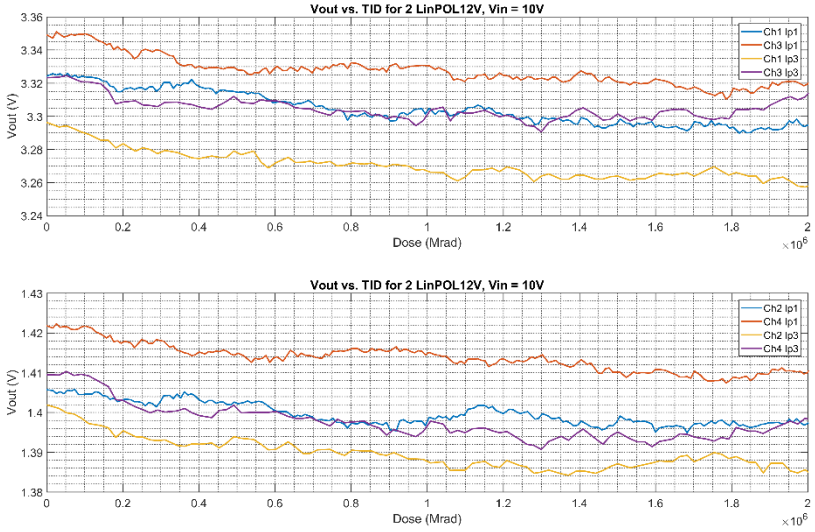
1. The output voltage of the regulators on 10 different LinPOL12V chips (each featuring two regulators providing respectively 3.3V and 1.4V) has been measured, in order to verify the chip-to-chip variations. The results (with Vin=8V and Iout=0A) are reported in the following graph:



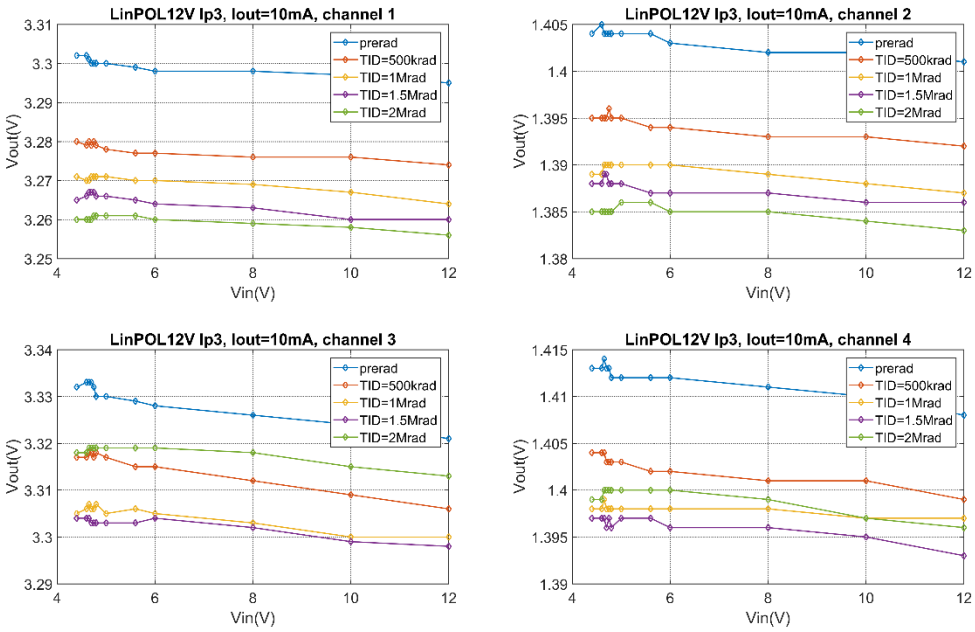
2. The line and load regulation of 4 different LinPOL12V (each featuring two regulators providing respectively 3.3V and 1.4V) has been measured (using Iout up to 30mA for Vout=3.3V, and up to 80mA for Vout=1.4V):



3. 4 LinPOL12V chips have been irradiated up to 2 Mrad at room temperature, using DR=0.576Mrad/h, Vin=10V, Iout=10mA. The evolution of the output voltages of the regulators with TID are shown in the following Figure:



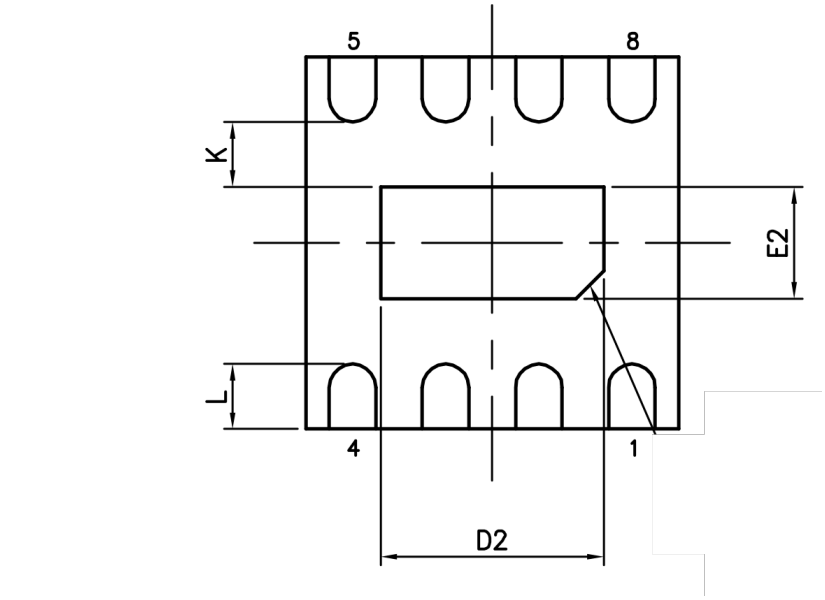
The line regulation has also been monitored during the irradiation, with Iout=10mA:



There is no TID-leakage induced peak on Vout* nodes with a minimum load of 1mA.

Package description

linPOL12V is packaged in a plastic Dual Flat No-Lead (DFN) package 2.0x2.0x0.9mm in size, with 8 pads and with an exposed pad to be soldered to the PCB for better thermal properties. The suggested PCB layout for the integration of linPOL12V is shown in the following figure. The dimension of the signal pads is 0.25x0.5mm and the one of the central exposed thermal pad is 1.6mmx0.9mm. All distances are referred to the center of the signal or exposed thermal pads.



JEDEC OUTLINE	MO−229		
PKG CODE	WDFN(X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.00 BSC		
E	2.00 BSC		
e	0.50 BSC		
K	0.20	—	—

D2 1.6mm
E2 0.9mm
Side dimensions 2x2mm

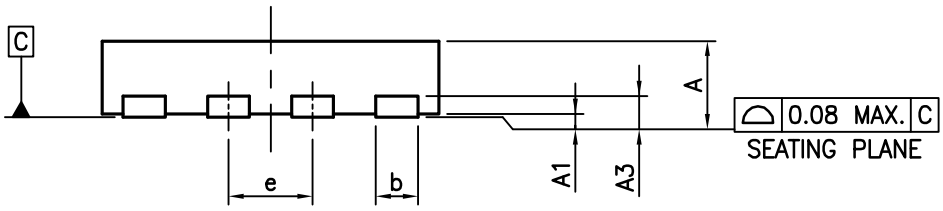


Figure 3: Suggested PCB layout for the integration of the linPOL12V DFN8 package.

Revision history

Revision	Date	Description
1.0	Nov 2017	First release of the document.
2.0	Jan 2018	Change of the pin number, now pin 1 is top left, before it was top right
3.0	Feb 2018	Change of the cavity dimension, package type DFN X208
3.1	March 18	Change of the block diagram, due to a mistake on Vin connection
3.2	Dec 2018	Change thermal pad dimension
3.3	Jan 2019	Added pull down resistor on _En* nodes and available test results
3.4	Aug 2022	Changed radiation tolerance results, waiting for ATLAS and CMS data