# bPOL48V

## GaN-based radiation and magnetic tolerant buck converter

**Features**
- GaN-based power stage.
- CERN-designed rad-hard CMOS controller ASIC.
- Input voltage range 17 to 48 V.
- Output current up to 10A.
- Integrated 5V and 12V regulators for the power stage.
- Adjustable switching frequency 0.5-3MHz.
- High bandwidth feedback loop (100KHz) for good transient performance.
- Under-voltage lockout.
- Over-Temperature protection.
- Power Good output.
- Enable Input.

**Applications**
Point Of Load in distributed power systems where radiation tolerance is required.

**Description**
bPOL48V is a 48V-input buck converter with 12V nominal (adjustable) output voltage, able to deliver up to 10A continuously. This converter is developed to provide an efficient solution for the distribution of power in High Energy Physics experiments and for space applications. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment.

bPOL48V is based on the CERN GaN controller, which has been developed to work seamlessly with the EPC2152 GaN ePower stage from EPC.

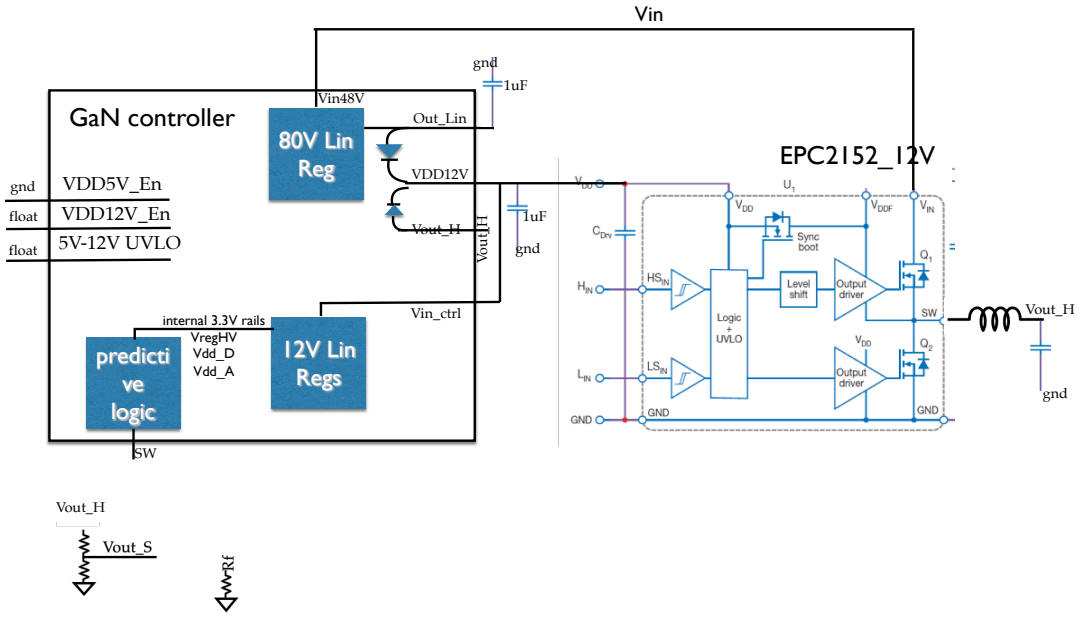
The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness by Design (RHBD) techniques, makes the controller capable of continuous operation up to very high radiation limit (50Mrad and 4e14 n/cm2 and 2.23e14 p/cm2(30MeV proton beam). GaN Controller has been designed for operation in a strong magnetic field in excess of 40,000 Gauss and has been optimized for air-core inductors of 200-500nH. To be compatible with these small inductance values, its switching operation is in the 0.5-3MHz range. Furthermore, the EPC2152 has been optimized to be radiation tolerant.

The controller integrates two linear regulators to generate of the supply voltage for the power stage without external active components: LinPOL48V and LinPOL12V. LinPOL48V output can be adjusted and has a nominal value of 12V, while LinPOL12V provides a fixed 5V output from 12V. Both regulators can be enabled separately.

bPOL48V protection features include Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions. The chip temperature increase in the application can be monitored via a dedicated analog signal (PTAT). A power good open drain output is available.

bPOL48V is particularly indicated for a conversion ratio 48V to 12V with a maximum output current up to 10A. The maximum suggested Vin voltage is 48V, reliability tests will be done.

## *Typical application*



# GaN Controller Specifications

## Absolute Maximum Ratings

Absolute maximum rating indicate limits beyond which damage to the device may occur and reliability may be compromised.

Input Voltage Vin48V……..……..…-0.3V to +50.0V
DiodeK……..……..…-0.3V to +70.0V
DiodeA……..……..…-0.3V to +70.0V
SW Voltage……..……..…-2.5 V to Vin+2.5V
SW_Clamp Voltage……..……..…-2.5 V to Vin+2.5V
Vout Voltage……..……..…0.3 V to 24V
OutLin Voltage……..……..…-0.3V to +14V
VDD12V Voltage……..……..…-0.3V to +13V
VDD5V Voltage……..……..…-0.3V to +5.5V
Vin control Vin_ctrl……..……..…-0.3V to +13V
Feedback input Voltage of the E/A Vi……..……..…-0.3V to +3.6V
Frequency selector Rf……..……..…-0.3V to +3.6V
VoutS voltage ……..……..…-0.3V to +3.6V
Buck_En ……..……..…-0.3V to +3.6V
Power good ……..……..…-0.3V to +3.6V
Current in PGood pin (when PGood is negated)……..…500uA
Feedback input Voltage of the E/A Vi……..……..…-0.3V to +3.6V
Frequency selector Rf……..……..…-0.3V to +3.6V
VoutS voltage ……..……..…-0.3V to +3.6V
Controller Enable ……..……..…-0.3V to +3.6V
Power good ……..……..…-0.3V to +3.6V
VDD5V_En ……..……..…-0.3V to +3.6V
VDD12V_En ……..……..…-0.3V to +3.6V

## Pin Configuration

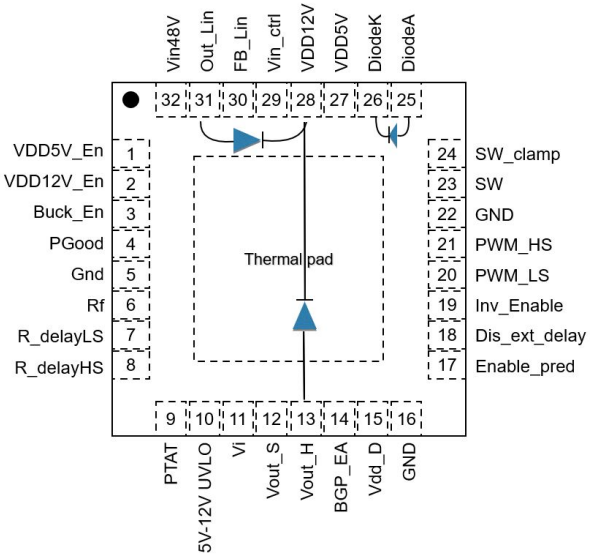


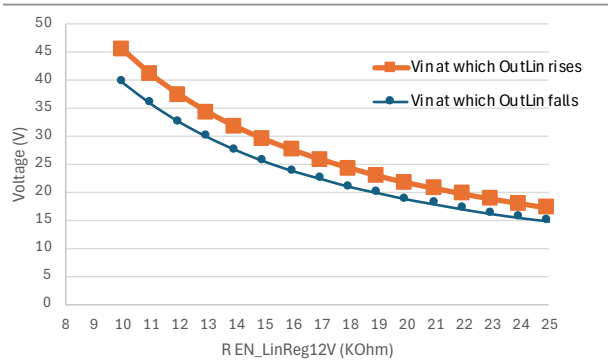

*Figure 1. Pin configuration*

## Pin Function

**VDD5V_En (Pin 1):** LinPOL12V (5V output) enable input. The linear regulator from the Vin_ctrl to 5V output is normally on, as this pin is connected to an internal pull-up at 3.3V. Connect this pin to ground to disable the regulator.

**VDD12V_En (Pin 2):** LinPOL48V (12V output) enable input. In order to ensure a proper startup in all conditions, a 24kΩ resistor from pin 2 to ground should be used. This resistor, in combination with the internal 500kΩ pullup resistor, enables LinPOL48V when Vin48V is above 17V, thus ensuring that Vin48V is above the minimum value. Connect this pin to ground to disable the regulator. It is not recommended to lower the value below 17V, but if the user would like to increase it, please follow the below plot and table to extract the right resistance for the wanted Vin enable value. Please consider that there is a hysteresis for turning on-off.

| R EN_LinReg12V (Kohm) | Vin at which OutLin rises (V) | Vin at which OutLin falls (V) |
|---|---|---|
| 10 | 45.15 | 39.55 |
| 11 | 40.75 | 35.75 |
| 12 | 37.15 | 32.55 |
| 13 | 34.05 | 29.85 |
| 14 | 31.45 | 27.55 |
| 15 | 29.25 | 25.55 |
| 16 | 27.35 | 23.85 |
| 17 | 25.65 | 22.45 |
| 18 | 24.15 | 21.05 |
| 19 | 22.75 | 19.95 |
| 20 | 21.55 | 18.85 |
| 21 | 20.55 | 17.95 |
| 22 | 19.55 | 17.05 |
| 23 | 18.65 | 16.25 |
| 24 | 17.85 | 15.55 |
| 25 | 17.05 | 14.95 |




**Buck_En (Pin 3):** Buck Enable input. GaN_Controller is normally disabled and requires a voltage above 800mV applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V. There is a hysteresis, to switch off GaN_Controller the Enable pin must be lower than 500mV. The polarity of the pin can be inverted by connecting Inv_Enable (Pin19) to gnd, in which case GaN_Controller is enabled for applied voltages below 800mV. Note that an embedded 500 kΩ resistor pulls the voltage of the Buck_En pin to gnd.

**PGood (Pin4):** Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when bPOL48V is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider, keeping the voltage in this pin below 3.3V. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 500uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disabled mode, during restart, in case of under-

voltage or over-temperature, and when the output voltage is outside a regulation window of approximately ±6.5% with respect to the selected Vout.

**GND (Pin 5,16,22):** Ground of the control electronics of the controller. It must be connected to the PCB ground power plane as close as possible to the power stage GND in a single point (star connection), in such a way to prevent high amplitude pulsed current to disturb the control circuit. Please refer to the recommended layout for further details.
**Rf (Pin 6):** Frequency Selector. A resistor placed between this Pin and the GND determines the switching frequency of the controller, as illustrated in the following table.

| Resistance (Ohm) | Frequency (MHz) |
|---|---|
| 270K | 1.03 |
| 200K | 1.35 |
| 180K | 1.48 |
| 160K | 1.65 |
| 130K | 1.99 |
| 100K | 2.51 |
| 82K | 2.98 |

**R_delayLS (Pin 7) and R_delayHS (Pin 8):** Resistors to set the dead time by defining the delays of the low side (td_OFF) and high side (td_ON) turn on times, if **Dis_ext_delay (Pin 18)** is set to GND. If **Dis_ext_delay (Pin 18)** is left floating, delay times are fixed internally to 25ns. The table below shows td_ON and td_OFF as a function of the resistors value.

| Rdelay [kOhm] | td_ON / td_OFF[ns] |
|---|---|
| 18 | 3.5 |
| 27 | 4,5 |
| 47 | 6,5 |
| 75 | 9,5 |
| 82 | 10 |
| 91 | 11 |
| 120 | 14 |
| 150 | 16,5 |

**PTAT (Pin 9):** Proportional-To-Absolute Temperature provides a voltage proportional to the variation of the chip internal temperature. The voltage at room temperature is around 500mV, with a large variability from chip to chip, the slope typical value is 8.5 mV/ºC.

**5V-12V UVLO (Pin 10):** UVLO level switch, internally pulled up to 3.3V. When this pin is floating, the UVLO levels are 10.5V in rising Vin_Ctrl and 9.5V for falling Vin_Ctrl. When this pin is connected to ground the UVLO levels are 4.5V and 4V. This pin, in combination with the 5V regulator, provides compatibility with power stages using 5V logic power supplies. Please contact dcdc.asic.support@cern.ch with details of the application to get detailed information for interfacing lower voltage power devices.

**Vi (Pin 11):** Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 100kHz, but the DC regulation voltage Vout is selected by the addition of 2 voltage dividers between Vout and gnd. The two voltage dividers are needed because the ESD protections connected to the feedback nodes can stand maximum 3.3V. A first Voltage divider (composed by Rout1 and Rout2) will scale down the Vout voltage to a "scaled" voltage Vout_S in a range between 1.5V and 3.3V. Vi is connected between the 2 resistors and the resulting voltage is compared to the internal reference voltage (about 580mV). The resistor between Vout_S and Vi must have a value of 1MΩ, while the one between Vi and gnd is selectable (no resistor makes Vout_S=Vref=580mV). Rout1 and Rout2 must be lower than 50KOhm in order to avoid issues in the compensation network. To set Vout=12V the following resistor values are recommended: Rout1=11KOhm, Rout2=3.3KOhm, Ri=262KOhm.
If Vout is below 3.3V the voltage divider Rout1/Rout2 is not required.

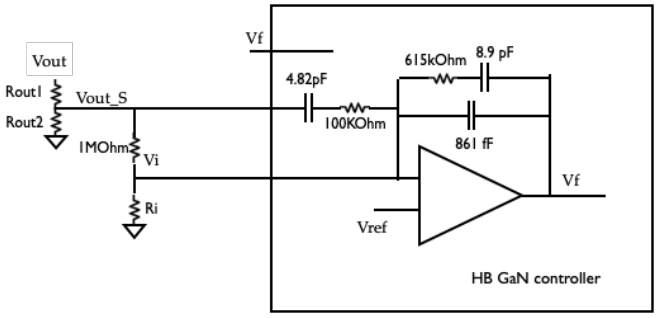



*Figure 2: Configuring the output voltage.*

**Vout_S (Pin 12):** Vout scaled down to a voltage below 3.3, to be compatible with the ESD protections. More information is reported in **Vi (Pin 11)** description**.**

**Vout_H (Pin 13):** Vout voltage recirculation input, connected to VDD12V through a diode. This connection allows to improve the efficiency by supplying the power stage from the output voltage, instead of using the linear regulator, when Vout is larger than OutLin. This methodology can be used only when Vout is set below 13V (to avoid exceeding the power stage maximum supply voltage) and Out_Lin lower than Vout using the resistor divider in FB_Lin (pin 32).

During the startup, when the output of the converter is low, the internal linear regulator will provide the 12V required trough the diode between Out_Lin and VDD12V. As soon as the output voltage becomes larger than Out_Lin VDD is supplied from Vout_H, which prevents unnecessary power dissipation in the linear regulator. In order to ensure that Vout takes over, Out_Lin should be set to approximately 10.5V for Vout=12V, please refer to FB_Lin (30) description.

If Vout recirculation is not used, this pin can be left floating.

**Bgp_EA (Pin 14):** The reference voltage to the Error Amplifier is buffered and made observable at this pin exclusively for test purposes. This pin should be left floating.

**Vdd_D (Pin 15):** internal voltage regulator outputs, made observable at this pin exclusively for test purposes. This pin should be left floating.

**Enable_pred (Pin 17):** To be connected to GND. This pin enables the predictive logic functionality to reduce the dead times automatically. This functionality requires several configuration changes, please contact dcdc.asic.support@cern.ch in case a fixed dead time is not suitable for your application.

**Dis_ext_delay (Pin 18):** If left floating, delay times td_ON and td_OFF are fixed internally at 25ns. If connected to gnd, the delay times are set by means of resistors in **R_delayLS (Pin 7)** and **R_delayHS (Pin 8).**

## GaN Controller Specifications (continued)

**Inv_Enable (Pin 19):** Connect to gnd to toggle the polarity of the **Buck_En (Pin 3)** pin. If not used, it is recommended to leave this pin floating.

**PWM_LS (Pin 20):** Low side (LS) gate signal to be connected to LSin pin of EPC2152.

**PWM_HS (Pin 21):** High side (HS) gate signal to be connected to HSin pin of EPC2152.

**SW (Pin23):** To be connected to PWM_HS (Pin 21) in normal operation.

**SW_clamp (Pin24):** To be connected to SW node. The clamping circuit draws current from this pin when the controller is disabled, to ensure that the output voltage does not rise uncontrolled when both HS and LS switches are off and there is no load connected to the converter. This pin has a resistive behavior with a slope of 4kΩ, and saturates at around 5mA when the voltage in the SW_clamp pin is greater than 20V. When the controller is enabled, the leakage current is smaller than 0.5µA. If not required by the application, this pin can be left floating.

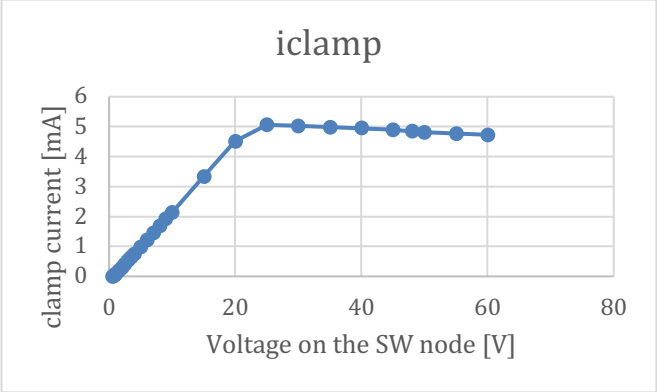



*Figure 3: Clamp current as a function of SW voltage. Controller disabled.*

**DiodeA (Pin25):** Anode of the floating diode. To be used as a bootstrap diode if a power stage without integrated diode is used.

**DiodeK (Pin26):** Cathode of the floating diode. To be connected to the Bootstrap capacitor. Please note that this pin experiences the bootstrap voltage with the high dynamics SW voltage superimposed, including the HS switch reverse conduction during td_ON, in case of negative inductor current. Therefore, to prevent overvoltage and ensure a reliable operation, an RC filter must be added to this pin, as shown on Fig. 4.

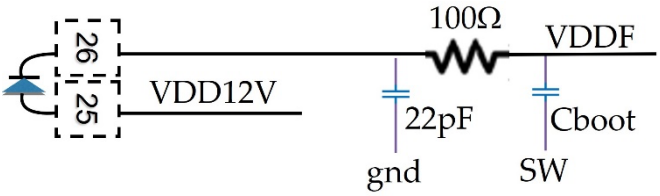



*Figure 4: Filter for high frequency spikes on DiodeK.*

**VDD5V (Pin 27):** Fixed 5V output of the 12V-input linear regulator. This regulator is provided for compatibility with GaN power stages using a 5V logic power supply. Please refer to **5V-12V UVLO (Pin 10)** description.

**VDD12V (Pin 28):** Please refer to **Out_Lin (Pin30)** specifications.

**Vin_ctrl (Pin29):** Supply voltage for the internal control circuitry. This pin is usually connected the same voltage as as the GaN power stage logic power supply (VDD12V pin). The 3.3V internal linear regulator starts up when Vin_ctrl is higher than 4.2V. The soft start procedure starts when the voltage on this pin is higher than the UVLO level configured by **5V-12V UVLO (Pin 10)**, and the **Buck_En (Pin 3)** is active.

**FB_Lin (Pin 30):** This is the feedback signal of the LinPOL48V linear regulator. It is internally connected to a voltage divider to regulate 12V in the Out_Lin pin as default. It can be overridden using an external voltage divider connected to VDD12V, as shown on the figure below. The voltage in the regulated point is:

VDD12V = Vref * (R1 + R2) / R2

With Vref = 1.22V typical.

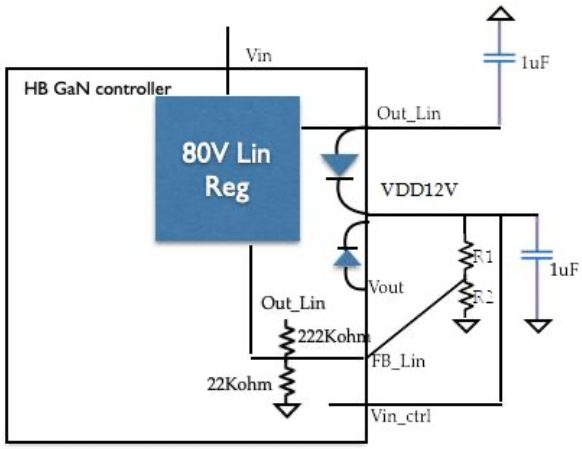



*Figure 5: LinPOL48V Configuration.*

**Out_Lin (Pin31):** Output of the linear regulator from Vin48V. The maximum current deliverable from this linear regulator is 100mA. A 1uF ceramic capacitor should be placed between Out_Lin and gnd (the maximum capacitive load of Out_Lin is 2uF).

**Vin48V (Pin32):** This input is connected to the LinPOL48V linear regulator, to internally generate the rest of the voltages for the controller and the supply of the EPC2152. It should be connected to the input voltage of the converter, with a decoupling 1uF ceramic capacitor placed as close as possible to the chip.

## GaN Controller Specifications (continued)

### Recommended Operating Conditions

| Description | Min | Max | Unit |
|---|---|---|---|
| Input voltage - Vin | 13 | 48 | V |
| Output voltage - Vout | 0.6 | 24 | V |
| Conversion ratio - Vout/Vin (min on time 40ns) | 2 | 20 | |
| Switching frequency | 0.5 | 3 | MHz |
| Cooling plate temperature (the power is dissipated trough the PCB by means of a cooling plate attached to its bottom side) | -40 | 50 | °C |
| Enable voltage | | 3.3 | V |
| Power Good voltage | | 3.3 | V |

### Electrical Specifications

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power** | | | | | | |
| Vin | Input voltage supply range | Controller operational | 13 | | 48 | V |
| Iin | Input current for control electronics (via Vin pin) | En pin low, controller disabled | - | 4.5 | - | mA |
| | | Enabled, 3MHz switching frequency | - | 6 | - | mA |
| **PWM** | | | | | | |
| DMax | Maximum Duty Cycle | | - | 97 | - | % |
| DMin | Minimum Duty Cycle | | - | 0 | - | % |
| ton min | Minimum on pulse width | Smallest PWM width (except 0ns) | | 40 | | ns |
| **Error Amplifier** | | | | | | |
| DCG | DC Gain | CL = 1pF at VF Pin | - | 90 | - | dB |
| UGBW | Unity Gain-Bandwidth | CL = 1pF at VF Pin | - | 20 | - | MHz |
| SR | Slew Rate | CL = 1pF at VF Pin | - | 10 | - | V/µs |
| **Under-Voltage Lockout** | | | | | | |
| VinStartTh | Vin to enable OutLin | Vin rising trip level, R=24kΩ between pin 2 and gnd | - | 17 | - | V |
| Vin_ctrl_Start_th | Vin_Ctrl to enable the internal 3.3V regulators. Rising | Vin_Ctrl rising trip level | - | 3.4 | - | V |
| Vin_ctrl_Stop_th | Vin_Ctrl to disable the internal 3.3V regulators. Falling | Vin_Ctrl falling trip level | - | 3.1 | - | V |
| **Enable** | | | | | | |
| EnStartTh | Enable start threshold | Enable rising trip level | - | 800 | - | mV |
| EnStopTh | Enable stop threshold | Enable falling trip level | - | 720 | - | mV |
| EnSerRes | Enable pin series resistance (to limit current through ESD when GaN_Controller is not powered) | | - | 10 | - | kΩ |
| EnPullDownRes | Embedded Enable resistor to GND | | - | 500 | - | kΩ |

## *GaN Controller Specifications (continued)*

| | | | | | | |
|---|---|---|---|---|---|---|
| **Protections** | | | | | | |
| OTPStartTh | Over Temperature Protection start threshold | Tj rising trip level | - | 120 | - | ºC |
| OTPStopTh | Over Temperature Protection stop threshold | Tj falling trip level | - | 80 | - | ºC |
| **SW_Clamp** | | | | | | |
| Iclamp | Clamping current | Controller disabled.<br>Voltage in the SW_Clamp pin = 2V | | 0.3 | | mA |
| Ileak | Leakage in the SW_Clamp pin | Controller enabled.<br>Voltage in the SW_Clamp pin = 60V | | 0.5 | | uA |
| **Soft Start** | | | | | | |
| SSt | Duration of the Soft Start procedure to reach regulation at nominal Vout | f=2MHz | | 400 | | us |
| | | f=3MHz | | 250 | | us |
| SSt_ton_min | Min on time of PWMHS during soft start | | 21 | | | ns |
| **Power Good** | | | | | | |
| OV | Output Over Voltage<br>PGood upper threshold | | | +6.5 | | % |
| UV | Output Under Voltage<br>PGood lower threshold | | | -6.5 | | % |
| **Proportional To Absolute Temperature signal** | | | | | | |
| PTAT | Analog output voltage | Controller disabled, environmental T sweep | | 8.5 | | mV/ºC |
| Rth | LinPOL48V thermal resistance to bottom side of PCB | Several loads. Temperature of the chip measured with PTAT and bottom plate temperature measured with thermocouple | | 10 | | ºC/W |

## *Radiation characteristics*

The waveforms and characteristics corresponding to the total ionizing dose (TID), single event effects (SEE) and displacement damage (DD) tests are shown in the **typical waveforms and characteristics** section.

## Block Diagram

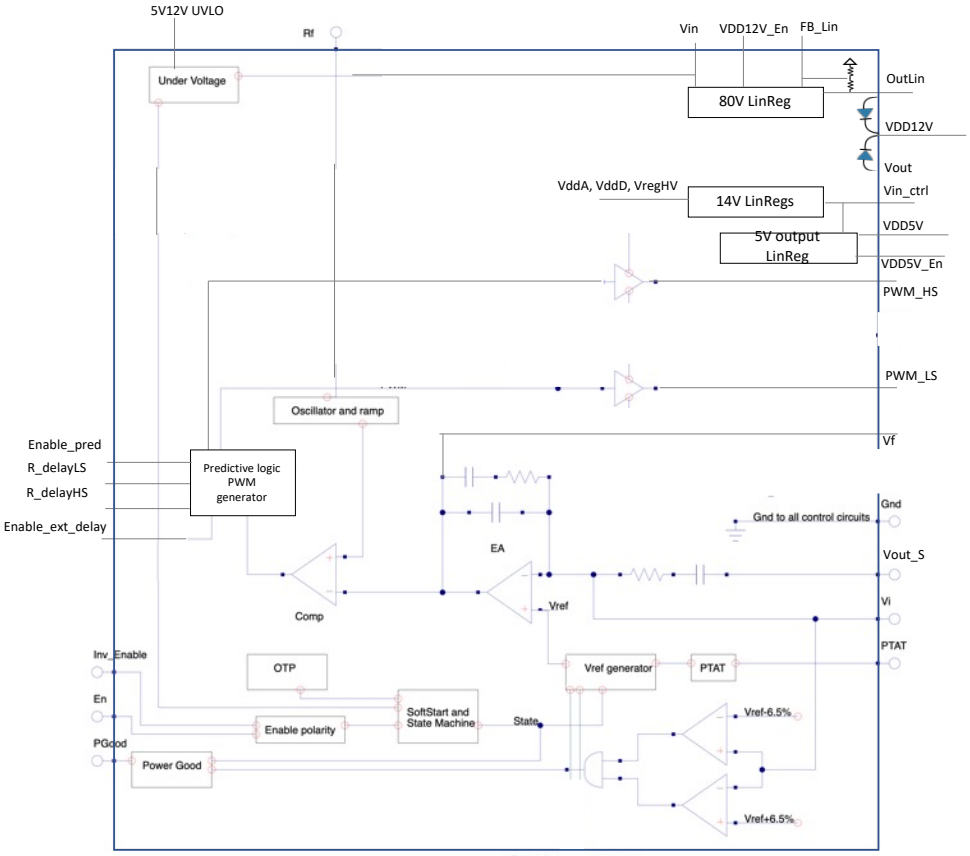



*Figure 6: Controller block diagram.*

## Package description

GaN_Controller is packaged in a 32pin plastic Quad Flat No-Lead (QFN) package 5.0x5.0x0.9mm in size, with an exposed pad to be soldered to the PCB for better thermal properties. The thermal resistance is between 27 to 31 ºC/W depending on the air flow.

The figures below show the package dimensions and recommended footprint.

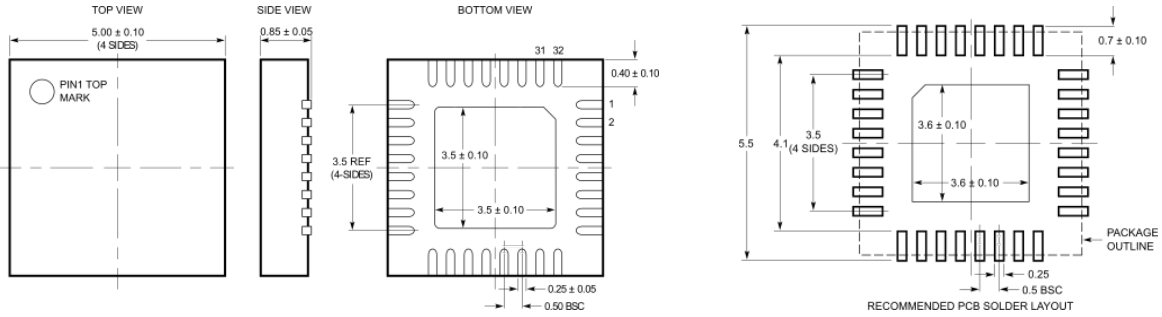



*Figure 7: QFN32 package dimensions for the controller.*

## GaN Controller Specifications (continued)

## Detailed description and operation

GaN_Controller is a half bridge buck converter controller explicitly designed to work with EPC2152 component, in high radiation and magnetic field environments such as High Energy Physics experiments or space applications. bPOL48V is the buck DCDC converter composed by GaN_Controller and EPC2152.

**Embedded linear regulators**
The GaN_Controller integrates all regulators required for powering the internal control electronics. Furthermore, two linear regulators LinPOL48V (48V-input) and LinPOL12V (12V-input) are integrated on chip to interface with the logic power supply of the GaN power stage. All storage capacitors required for the internal control regulators are on-chip and have been sized to ensure steady voltage even during large current surges. LinPOL48V and LinPOL12V require 1uF and 10uF external ceramic capacitors, respectively, placed as close as possible to their output pins.

**Control electronics Under-Voltage lockout**
The embedded linear regulators need a sufficient headroom voltage to provide stable voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when Vin_Ctrl is above about 3.4V (on rising Vin_Ctrl). This comparator has a hysteresis, and the linear regulators are disabled again when, for falling Vin_Ctrl, when Vin_Ctrl drops below about 3.1V.

**GaN_Controller Under-Voltage lockout**
EPC2152 has an embedded VDD UVLO and to ensure proper working functioning of the EPC2152, the controller enter in soft-start procedure only when Vin_Ctrl (which is normally shorted with EPC2152's and HB_GaN_Controller's VDD) is above 10.5V in rising edge.
The comparator which is used to define this threshold has a hysteresis and the GaN_Controller is turned off when, for falling Vin_Ctrl, Vin_Ctrl drops below about 10V.

**Enabling HB_GaN_Controller**
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has not been asserted by applying a voltage above about 800mV. The Enable pin has a hysteresis of 300mV, therefore GaN_Controller will turn off when Enable pin's voltage is under 500mV. GaN_Controller can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each GaN_Controller providing regulated power to a different load). GaN_Controller is disabled by default if the En pin is floating – an internal pull-down resistor of 500 kΩ keeps the voltage of the pin to gnd.
The polarity of the enable signal can however be inverted by connecting the Inv_Enable pin to gnd. In this case, the circuit is disabled when a voltage above 800mV is applied to the enable (En) pin, and vice versa the circuit is enabled when a voltage below 500mV is applied; it is hence enabled by default if the En pin is floating – an internal pull-down resistor of 500 kΩ keeps the voltage of the pin to gnd.

**Soft Start procedure**
When bPOL48V converter (GaN_Controller and EPC2152) is enabled, a large current is required to charge the output capacitors to the nominal regulated voltage. This current must be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the Error Amplifier (EA). The output voltage reaches the nominal value in about 400us when using 2MHz switching frequency and 250us for 3MHz switching frequency. Every time the controller is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small overshoot in Vout at the end of the SS procedure.

**Power Good flag**
The PG output pin is used to signal that GaN_Controller is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 3.3V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the controller is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in reset and when the output voltage is outside a ±6.5% window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (via a voltage divider, maximum 3.3V). Current in the NMOS pull-down transistor must be limited below 500uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PG pin is 3.3V.

**Over-Temperature Protection (OTP)**
A dedicated circuit monitors the on-chip junction temperature and disables GaN_Controller when it reaches about 120ºC. The OTP has a hysteresis of about 40ºC, hence the controller restarts (with SS) when the junction temperature decreases below 80ºC. In case of inefficient cooling, it is hence possible that the controller cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

**Predictive logic**
GaN_Controller provides a predictive logic for minimizing the dead time. This logic senses the phase voltage to monitor the diode conduction, both in continuous and Quasi Square Wave (QSW) operation, characterized by negative inductor current (when Low Side switches off). The predictive logic reduces the internal 25ns fixed delay at startup, in order to achieve around 10ns diode conduction time. This functionality is useful if a large drift in the switches delay is expected over the operation range. However, as it requires several configuration changes, please contact dcdc.asic.support@cern.ch for instructions on how to enable it.

**Compensation network**
The compensation network is fully integrated and determines a typical loop bandwidth of about 100kHz in the recommended operation environment (frequency, voltages, inductor, on-board passives). GaN_Controller is hence capable of quickly adjusting the output voltage in case of output load transients.

**Cooling**
GaN_Controller contains a linear regulator which could dissipate a large amount of power depending on the conditions. VDD of EPC2152 could require 30mA, which produces a power dissipation in the order of 1.5W for 48V input voltage and 12V output. The QFN32 package has an exposed cooling pad to which the IC is directly attached. This pad must be soldered to the gnd plane of the PCB which itself must have a good thermal contact to the cooling system.

**Proportional To Absolute Temperature (PTAT) voltage**

The PTAT analog signal can be used to monitor the temperature (T) rise of the GaN_Controller ASIC during operation, to verify that the cooling is appropriate. The absolute value of the PTAT voltage at a given T has a wide sample-to-sample variability. However, the PTAT increase with respect to T is very close to a straight line with slope 8.5 mV/ºC. This linear relation is shown for one of the measured samples in the figure below from previous prototypes in the same technology. The discontinuity above 100ºC happens when the OTP sets in and is due to a hysteresis inserted because of the over-T protection. The vertical scale has an origin at about 25ºC in this case because the PTAT variation has been arbitrarily referred to the value at that T. Given the variability in the absolute value of the PTAT, it is possible that some sample outputs a 0V signal for very low T and only start to the linear relation at higher temperature. In our tests, this happened in one sample (0V output between -30 and -18ºC).

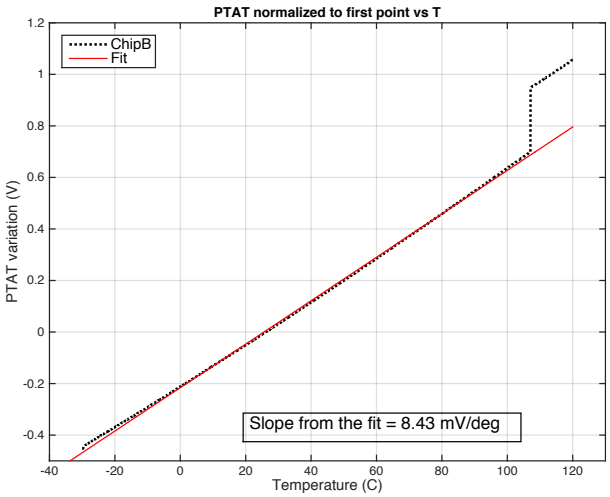



*Figure 8: PTAT voltage vs Temperature.*

## *bPOL48V design guidelines*

This section presents the guidelines for the design of the rad-hard buck converter bPOL48V. The design files of the module can be shared upon request to dcdc.asic.support@cern.ch. It is strongly recommended to use the validated design, as it was explicitly designed and optimized to ensure stability, performance and long-term reliability of both the controller and the GaN Power Stage.

Figure 9 shows the block diagram of bPOL48V. The most relevant design criteria of each block will be described in this section.

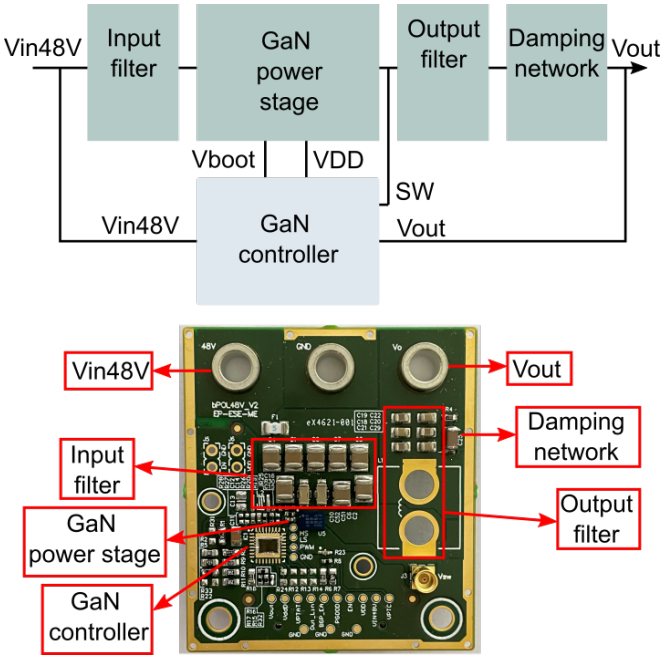



*Figure 9: bPOL48V block diagram (top) and PCB (bot)*

**Input filter and GaN power stage**

The input filter serves two purposes: input voltage and current ripple reduction, and voltage stress reduction on the power devices. The input power loop in a Buck converter is shown on Fig. 10, it is formed by the loop between the input capacitors Cin and power switches Sw1 and Sw2. This loop presents a trapezoidal-shaped current with fast edges that, in combination with the parasitic inductances highlighted in red, could create high amplitude voltage transients and oscillations.

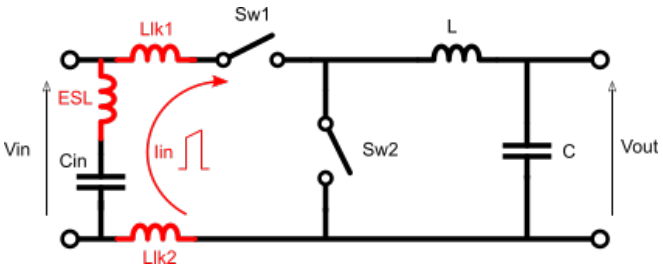



*Figure 10: Input power loop parasitic inductances.*

In order to have a reliable operation, the parasitic inductances of the board and packages (Llk1 and Llk2) and the ESL of the input capacitors should be reduced as much as possible.

The ESL reduction can be achieved by the proper selection of the technology and package of the capacitors. For bPOL48V, a combination of high capacitance bulk capacitors for ripple reduction and high frequency capacitors is required. For the bulk capacitance, using several 2.2uF 100V-rated ceramic capacitors is recommended. For the high frequency filtering, low ESL capacitors such as Murata NFM31KC104R2A3L should be placed as close as possible to the input power pins of the GaN power stage.

The reduction of the board parasitic inductance is achieved by generating a vertical power loop and reducing as much as possible the distance between the top and internal layers, as shown in Fig. 11. The recommended dielectric thickness between top and the first internal is 100um.

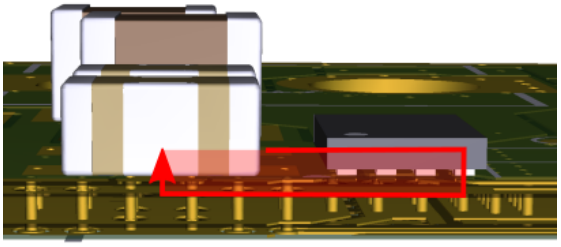


*Figure 11: High frequency power loop.*

Furthermore, the return GND path on the first internal layer (Layer 1) should be a solid uninterrupted plane. Therefore, if mechanical through-hole vias are used, it may be necessary to remove the unused pads to meet minimum trace width between vias, as shown in
Fig. 12.

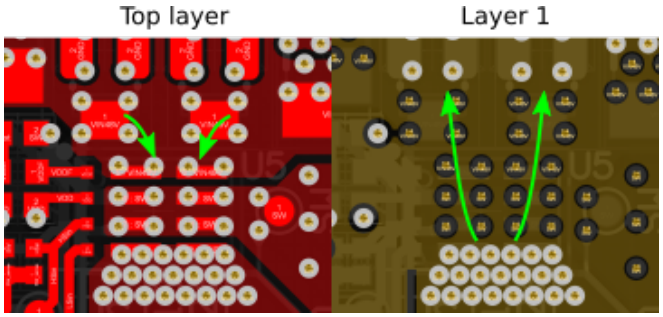



*Figure 12: Power planes recommendation.*

By following the above recommendations, the input power loop inductance is lower than 150pH. This value has been obtained by simulating the physical board on the Ansys SIwave software and later confirmed experimentally.

**Output filter and damping network**

The output filter is composed by a filter inductor and capacitors. The filter inductor defines the current ripple amplitude in combination with the switching frequency, input and output voltages, and it has a direct impact on the system efficiency. bPOL48V has been tested and optimized for two configurations: one using a 220nH air core inductor for High Energy Physics applications, where the converter must operate in a high magnetic field environment, and the other using a 1uH ferromagnetic inductor for applications without magnetic field restrictions.

Furthermore, given that the resonance between the inductor and filter capacitors could produce instabilities in the voltage control loop, a RC damping network should be added to the output to reduce the resonance peak and avoid oscillations in the output voltage.

The table below shows the recommended value of the output filter components and switching frequency (fsw) for each configuration, where L is the value of the filter inductor; Cout is value, type and quantity of capacitors in parallel for the output filter capacitor; Rdamp is the value of the damping resistor and Cdamp is the value, type and quantity of capacitors in series with Rdamp. For stability reasons, the cutoff frequency of the LC filter should be between 30kHz and 50kHz, considering the real capacitance of Cout due to the dc bias of the ceramic capacitors.

The recommended fsw maximizes efficiency for the selected inductor value.

| L | 220nH | 1uH |
|---|---|---|
| Cout | 12x 22uF 25V 0805 MLCC | 12x 10uF 25V 0805 MLCC |
| Rdamp | 0.1Ω 0603 | 0.1Ω 0603 |
| Cdamp | 2x 47uF 16V 1210 | 2x 47uF 16V 1210 |
| fsw | 2MHz (Rf = 130kΩ) | 1MHz (Rf = 270kΩ) |

It is recommended to use as many capacitors in parallel as possible for Cout to reduce the ESL as much as possible, thus improving the filtering performance.

**GaN controller and supply of GaN power stage**

As previously described, the GaN controller integrates all linear regulators required to supply the internal electronics and the external GaN power stage from the 48V input voltage (Vin48V).

The output of linPOL48V linear regulator (OUT_LIN) is internally connected to VDD12V pin through a diode. VDD12V is then used to supply the control electronics, via the VIN_CTRL pin, and the GaN power stage VDD. It is recommended to use an LC filter between VDD12V and VDD in order to filter out possible transients produced by single event effects. The recommended values are 20nH (part number 0806SQ-19NGLC, if air core is required) and 22uF ceramic capacitor. Furthermore, for the VIN_CTRL input, a 100nF capacitor is recommended as close as possible to the pin.

In order to ensure a proper start up of the converter, a diode has been integrated on the controller in order pre-charge the bootstrap capacitor. Please follow the recommendations described in the "pin function" section for pin 26 (DiodeK).

**Additional layout recommendations**

The GaN controller is provided in a QFN-32 package with an exposed pad in the bottom. This pad should be soldered to the ground plane, using many vias to provide good thermal transfer to the bottom side of the board. Using 17 filled and capped vias, 0.35mm hole diameter, spaced 1mm in the horizontal axis and 0.7mm in the vertical, with an interleaved arrangement yields approximately a thermal resistance of 10 ºC/W for the linear regulator (from PTAT measurement to bottom plate temperature).

It is recommended to use the second layer as a ground plane. The signal ground (controller) and the power ground should be connected on a single point, preferably at the logic input pins of the GaN power stage. This recommendation is aimed to prevent ground voltage bouncing on the controller due to the high magnitude current ripple in the power stage.

**Reliability**

Reliability has been assessed building a dedicated rack hosting 60 converters working continuously with Vin=48V, Vout=12V, L=220nH, fs=2Mhz, Iout=5A. The converters are enable/disabled every 1h. The rack is still running and on Nov 2024 60 converters worked for 4300h without failure. Regular updates will be provided in meetings and datasheet.

## *Typical waveforms and characteristics*

Full characterization of the bPOL48V is ongoing, following plots are from preliminary results.

### Switching characteristics

Figure 13 shows the switching node voltage characteristics for two different load conditions, when using the PCB layout recommended in the design guidelines. When Iout = 5A the inductor current is negative on the switch off instant of the low-side GaN FET, which causes the high-side GaN FET to conduct in reverse during the dead time. The reverse conduction voltage in this condition adds to the switching node voltage above the Vin value. When Iout = 10A, the converter operates with hard switching in all transistors.

As it can be seen, there are no overvoltage spikes due to the optimization of the switching speed of the EPC2152 GaN power stage and the PCB layout.

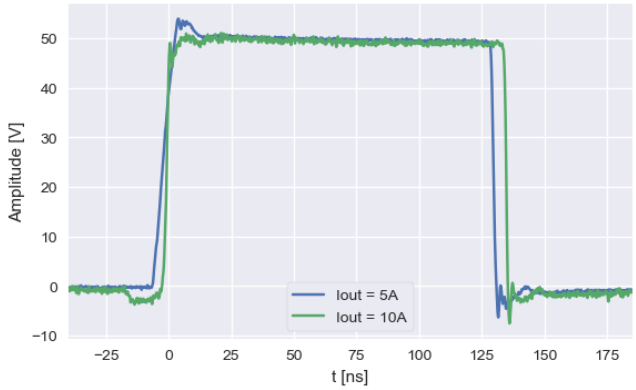



*Figure 13: Switching node waveforms. 220nH inductor, 48Vin, 2MHz.*

### Efficiency

#### Efficiency for 220nH air core inductor

The 220nH air core inductor has been built using Litz Wire (1125 x 0,071mm P155 from Elektrisola, total section 4.45mm$^2$) on a toroidal plastic core. This inductor is a custom design for the prototype, and it is not provided. Nevertheless, the design details are available upon request to dcdc.asic.support@cern.ch.

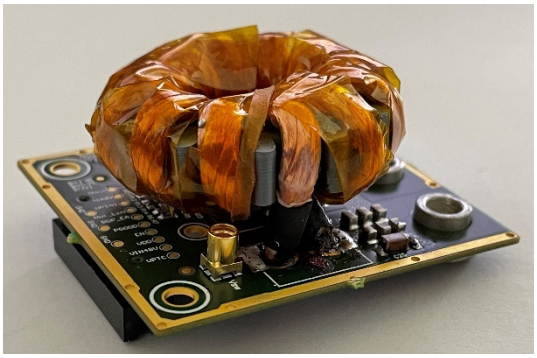


*Figure 14: bPOL48V with air-core 220nH inductor.*

bPOL48V has been tested for different input voltages in the recommended configuration, detailed in the design guidelines section, up to Iout = 13A. The cooling of the converter has been performed from the bottom of the PCB, with a cooling plate temperature between 20 ºC and 30ºC.

The efficiency is show in Fig. 15. It should be noted that, depending on the load and input voltage, the converter operates with the high side switch in zero voltage switch-on (QSW) or hard switch-on. The change in the operating mode is indicated with different markers on the figure.

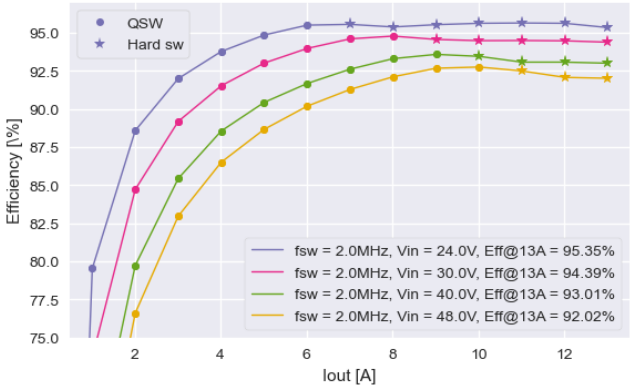



*Figure 15: Efficiency 220nH air-core inductor.*

#### Efficiency for 1uH ferromagnetic core inductor

For the case of the 2.2uH ferromagnetic inductor, the part number IHLP6767GZER2R2M01 was used. The resulting efficiency is shown in Fig. 16 for different input voltage values and load condition up to 13A, using the recommended configuration in the design guidelines section.

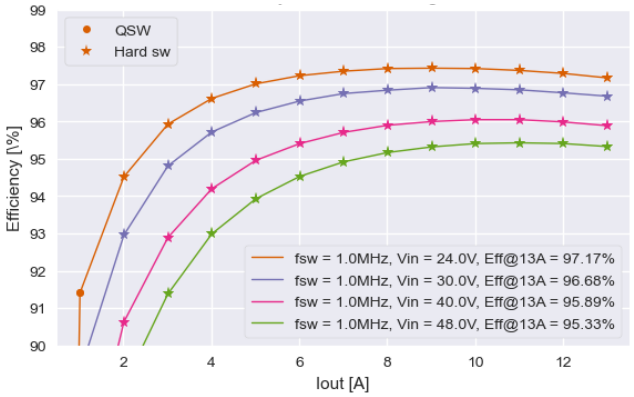



*Figure 16: Efficiency 1uH ferromagnetic core inductor.*

**Efficiency for 460nH air core inductor, Vout = 2.5V**

In this configuration, the bPOL48V has been tested for the load conditions of the first stage of point of load converters: Vout=2.5V and up to 5A load current. The tested input voltages are 12V, 20V and 24V.
The figure below shows the picture of bPOL48V using a toroidal air core inductor. The size of the board could be significantly reduced if this power level is required by reducing the number and footprint of the input and output capacitors, which, in this prototype, are rated to a higher voltage and sized to filter larger current ripples.

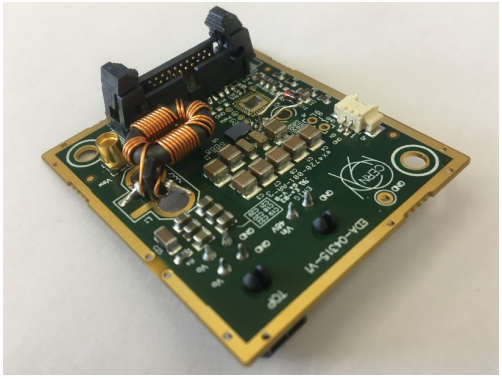


*Figure 17. bPOL48V using the FEASTMP inductor.*

Figure 18 shows the efficiency when using this configuration and fsw=2MHz. As it can be seen, the converter is suitable to be used for Vin up to 24V. The minimum input voltage is 12V, to ensure the correct voltage supply for the EPC2152 logic and driving stages.

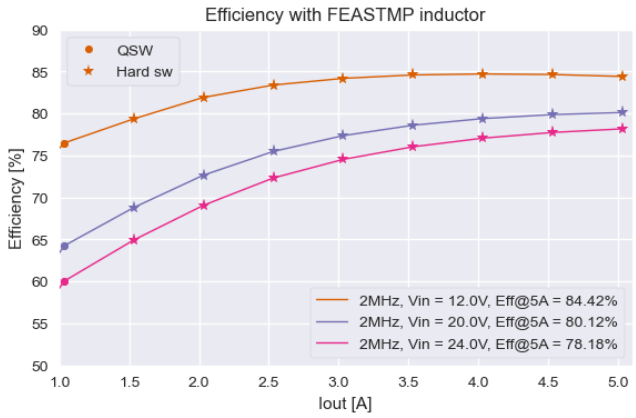
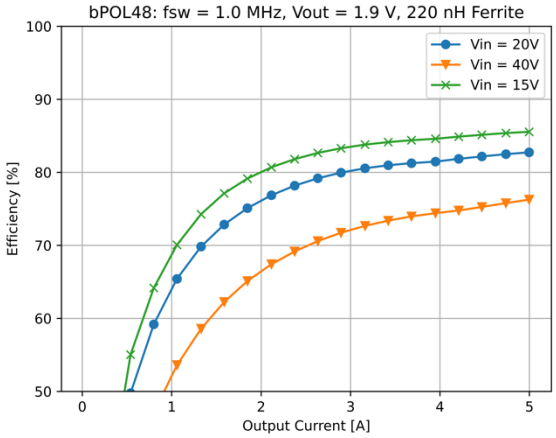
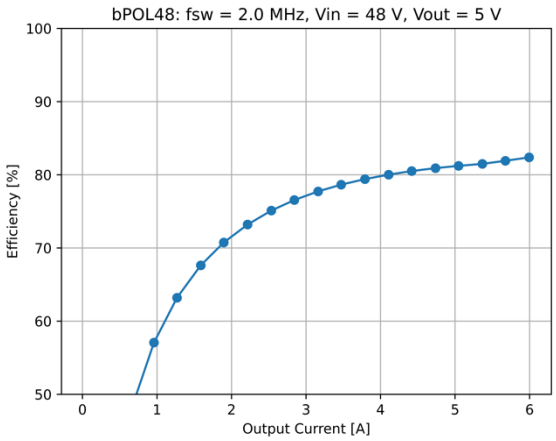



*Figure 18. Efficiency of bPOL48V with 460nH small air-core inductor and Vout=2.5V.*

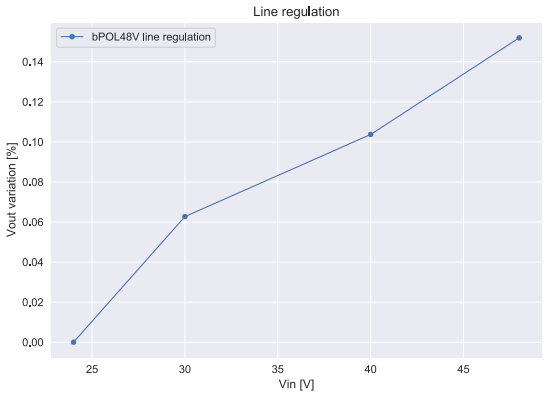
**Efficiency for different Vout**
The following figures show the efficiency when using this different Vout (1.9V and 5V), using configurations that are reported in the title of the picture.

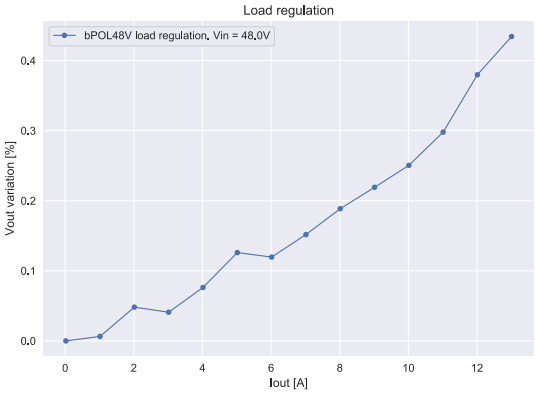



**Line and load regulation**

The following figures show the line and load regulation of the bPOL48V. The result is given in % of the output voltage. The configuration used is 2MHz, 460nH air core, Vout=12V,Vin=48V (for the load regulation) and Iout=5A for the line regulation.






## Radiation tolerance

**TID – Total Ionizing Dose**

bPOL48V with the 220nH inductor configuration has been irradiated with x-rays to study the TID effects, using the X-ray irradiation system at CERN. This system is the Seifert RP149, part of the CERN-EP-ESE equipment, which is routinely used for TID tests of deep submicron technologies. With a 50kV-3kW tube, a tungsten target and a 150µm thin Al filter, it produces an X-ray spectrum that has been well characterized in literature and is well accepted by the radiation effects community.

Figure 19 and Figure 20 shows the Vout vs TID when testing at room temperature and at -30ºC, respectively. As it can be seen, both figures have two x-axes, the top one indicates the dose deposited on the GaN EPC2152 and the bottom one indicates the dose on the Si controller. The test at room temperature was conducted up to a TID of 228 Mrad for the controller and 432 MRad for the GaN power stage. As it can be seen, there is no significant change in the output voltage due to radiation up to the tested dose. All other variables such as internal regulators, PTAT signal, bandgap and efficiency are also stable and close to pre-rad specifications up to the reached TID.

The test at -30ºC was conducted up to a TID of 67 Mrad for the controller and 126 MRad for the GaN power stage. The temperature control was done on the coldplate in which the converter is mounted, so the actual temperature on the controller and power stage is larger. Similarly to the ambient temperature test, there is no significant change in the output voltage due to radiation up to the tested dose. All other variables such as internal regulators, PTAT signal, bandgap and efficiency are also stable and close to pre-rad specifications up to the reached TID.

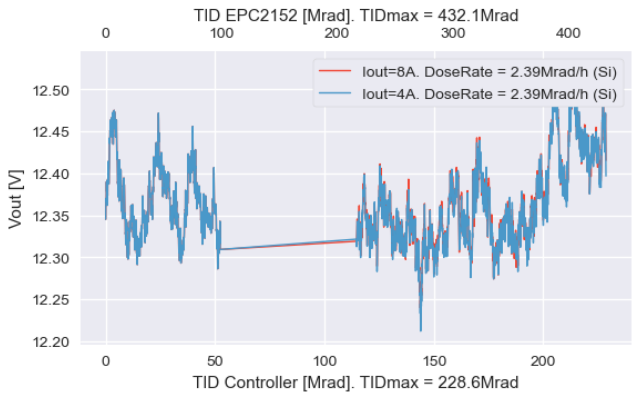



*Figure 19. bPOL48V Vout vs TID. Ambient temperature.*
*Note: Acquisition failed between 52MRad and 114MRad*

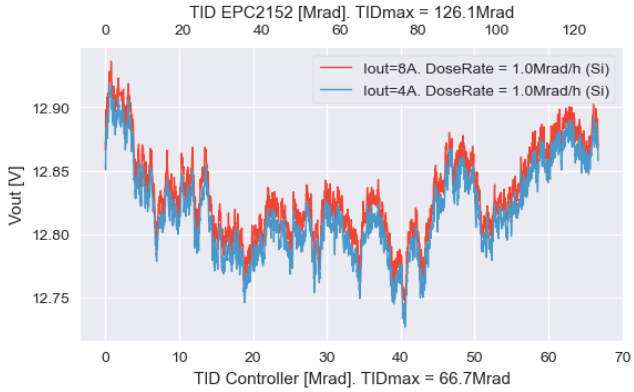



*Figure 20. bPOL48V Vout vs TID. -30ºC temperature.*

**SEE - Single Event Effects**

The single event effects (SEE) have been evaluated for the controller using heavy ions on the bPOL48V in the Cyclotron Resource Center of UCLouvain. In these tests, the effect on the EPC2152 is negligible, as the range of the heavy ions is not large enough to deposit charge on the sensitive area of the EPC2152. The GaN power stage is being characterized by EPC Co.

Figure 21 shows the single events transients on Vout for different linear energy transfers (LET). The transients have been divided in two types depending on the sign of the variation with respect to the average value: Type-0 when the transients are negative, and Type-1 when the transients are positive. An example of the shape of these transients is shown on the right part of the figure. The left part of the figure shows the distribution of the amplitude (in absolute value), for each LET. The x-axis label also shows the number of events and the reached fluence for each case.

The ions and tilt angles corresponding to each of the tested LETs are listed on the table below.

| Ion | Tilt angle [degrees] | Equivalent LET (Si) [MeV/(mg/cm²)] |
|---|---|---|
| $^{36}Ar^{11+}$ | 0 | 9.9 |
| $^{36}Ar^{11+}$ | 45 | 14 |
| $^{58}Ni^{18+}$ | 0 | 20.4 |
| $^{103}Rh^{11+}$ | 0 | 46.1 |
| $^{103}Rh^{11+}$ | 45 | 65.2 |
| $^{124}Xe^{35+}$ | 0 | 62.5 |
| $^{124}Xe^{35+}$ | 45 | 88.4 |

bPOL48V was tested up to LET = 88.4 MeV/(mg/cm²), no destructive events have been observed. In general, the amplitude of the transients increases with increasing LET. The maximum amplitude is around 25% for the Type-0 events, in rare cases and for LET > 62.5 MeV/(mg/cm²).

For High Energy Physics (HEP) applications, where statistically most of the events have LET<15 MeV/(mg/cm²), the maximum negative transient amplitude (Type-0) is below 10% and there are no positive events (Type-1).

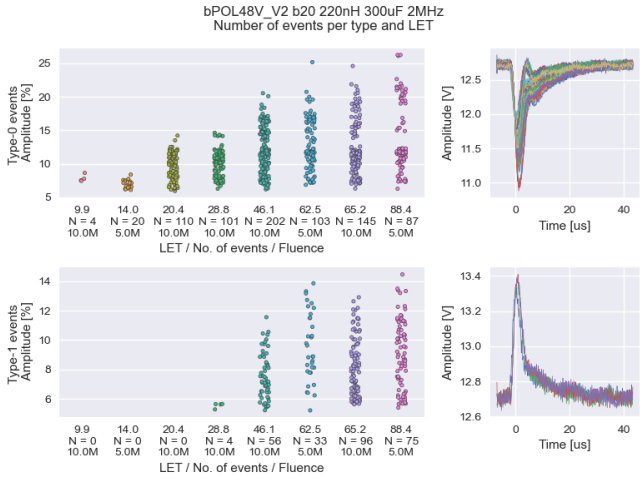



*Figure 21. Single Event Transients*

**DD -Displacement Damage**

For displacement damage (DD), the controller has been tested with 25MeV protons in the MC40 Cyclotron Facility in Birmingham and Neutrons in the TRIGA reactor in Ljubljana. There is no degradation for fluences up to 2.23E14 p/cm$^2$ and 4E14 n/cm$^2$.

For the case of the EPC2152 GaN power stage, it has been irradiated with 24GeV protons in the IRRAD facilities at CERN and neutrons in the TRIGA reactor in Ljubljana. There is no degradation for fluences up to 2.5E15 p/cm$^2$ and 1E15 n/cm$^2$.

## *Revision history*

| Revision | Date | Description |
|---|---|---|
| 0 | June 2020 | First release of the document, preliminary datasheet |
| 1 | May 2021 | Test results updated |
| 2 | May 2022 | bPOL48V V2.1 updates |
| 3 | Aug 2022 | Typical application and description updated |
| 4 (V2.2) | Aug 2022 | Updated recommended configurations and description |
| 5 | Aug 2022 | Added package thermal information for linear regulator |
| 6 (V2.3) | Nov 2022 | Updated recommended value of ferromagnetic inductor |
| V2.4 | Jun 2024 | Updated resistance values for VDD12V_En pin, updated Efficiency curves for different Vout and added line and load regulation |
| V2.5 | Nov 2024 | Updated reliability results |