bPOL2V5_V3.3

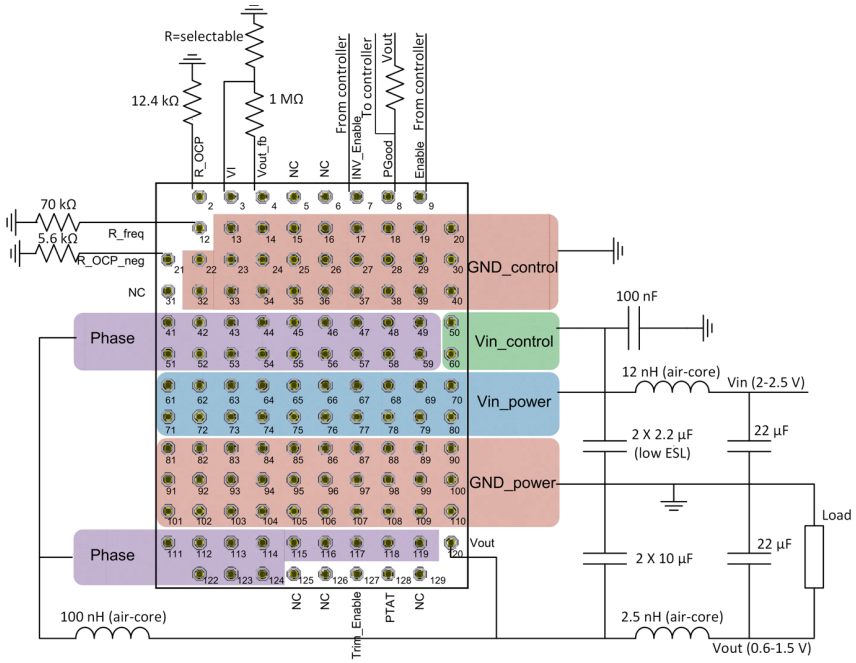
Radiation tolerant Synchronous Step-Down Buck DC/DC converter

Features
- Input voltage range 2.1 to 2.5V
- Output voltage range 0.6 to 1.5V
- Continuous 3A load capability
- Integrated N- and P-channel MOSFETs
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (190KHz) for good transient performance
- Positive and negative Over-Current protection
- Under-voltage lockout
- Soft-Start
- Power Good output
- Enable Input
- Radiation tolerance: tested for Total Ionizing Dose up to 100 Mrad (SiO_2), for Single Event Effects up to a Linear Energy Transfer of 40 MeVcm^2/mg and for Displacement Damage up to 2e16 n/cm^2. A previous prototype (bPOL2V5_V3.1) was tested for Displacement Damage up to 6.6e15 p/cm^2.

Applications
Point of Load (PoL) in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

Description
bPOL2V5_V3.3 is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes bPOL2V5_V3.3 capable of continuous operation up to 100Mrad (SiO_2) of Total Ionizing Dose. Single Event Effects resilience has been also targeted, and bPOL2V5_V3.3 has been irradiated with heavy ions up to a Linear Energy Transfer of 40 MeVcm^2/mg, showing no destructive SEEs or output power interruptions. Concerning displacement damage, neutron and proton irradiations showed that the converter is tolerant to a total fluence of respectively 2e16 n/cm^2 and 6.1e15 p/cm^2. bPOL2V5_V3.3 has been designed for operation in a strong magnetic field in excess of 40,000 Gauss, and has been optimized for air-core inductors of 80-120nH: to be compatible with these small coil values, its switching operation is in the 3-4.5MHz range.
The monolithic construction of bPOL2V5_V3.3, with the integration of the power train, makes the converter a space-efficient solution to provide PoL regulation from a 2.5V supply rail. Its protection features include negative and positive Over-Current, Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions.
bPOL2V5_V3.3 is a bump bonded ASIC which is meant for chip-on-board mounting. It requires via-in-pad and a specific layout of the board

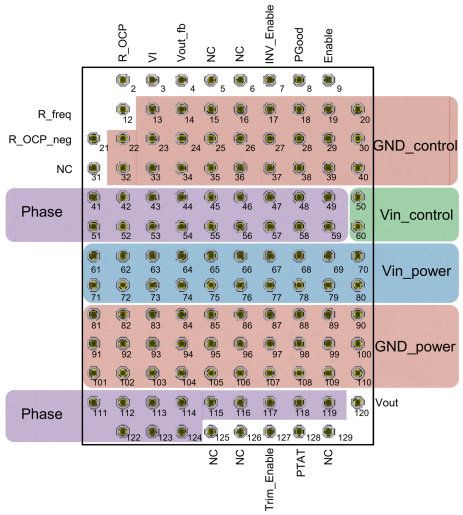
Typical application



Absolute Maximum Ratings

Power Input Voltage Vin_power…..……..…..-0.3V to +2.5V
Control Input Voltage Vin_control……..…….. -0.3V to +2.5V
Phase Voltage…..-0.3 V to Vin (DC), -0.8 to 3.4 V (AC, 10ns)
Feedback input Voltage Vi……..……...-0.3V to +1.32V
Converter Enable En ……..……..……..-0.3V to +2.5V
Power good PGood……..……...……-0.3V to +2.5V
Output Voltage Vout……..……-0.3V to +2.5V
Current in PGood pin (when PGood is in logic state '0')..50uA

Pin Configuration *(top view, as on landing pattern for PCB)*



Pin Function

R_OCP (Pin 2): Positive over-current protection limit selector. A resistor placed between the R_OCP pin and the board ground determines the limit of the positive overcurrent.
Concerning the positive over-current limit, the default resistance of 12.4 kΩ fixes the maximum instantaneous inductor current to a typical value of OCP_pos=4.7 A: the corresponding load current $Iout_{OCP}$ at which the protection is triggered can be estimated as:

$$Iout_{OCP} = OCP\_pos - (Vin\text{-}Vout)(Vout/Vin)/(2Lf_{sw}),$$

where L is the inductor value and f_{sw} is the switching frequency. $I_{out,OCP}$ is thus around 3.9 A with Vin = 2.5 V, Vout = 1.2 V, f_{sw} = 4 MHz and L= 100 nH.

Vi (Pin 3): Input voltage of the Error Amplifier. The control loop makes the DC value of this node equal to the internal reference voltage, which is 300 mV ± 1mV. The DC regulation voltage Vout is selected by means of two external resistors (R1 and R2 in Figure 1), forming a voltage divider between Vout_Fb and the board ground. The intermediate node of such voltage divider is connected to Vi. R1 must have a value of 1 MΩ, while R2 is selectable to obtain the desired Vout (in the range 0.6-1.5 V):

$$Vout \approx 0.3\ (R1+R2)/R2$$

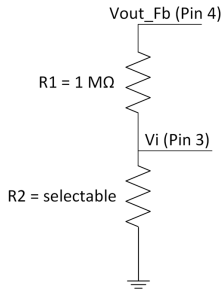


Figure 1: Configuring the output voltage.

Vout_Fb (Pin 4): Regulated output voltage. This is an input pin allowing the connection of Vout to the control loop of the converter. It must be connected as specified in the description of Pin 3 (Vi). Vout_Fb is connected to the Vout pin (Pin 120) through on-chip metal lines. The positioning of the Vout_Fb and Vout pins is studied to allow easier integration on the PCB, as the Vout pin has to be connected to the output capacitor, while placing Vout_Fb close to Vi is beneficial, as resistor R1 must be connected between these two pins.

INV_Enable (Pin 7): Toggle of the polarity of the Enable pin. If this pin is connected to ground, the polarity of the Enable pin is switched. It is recommended to leave this pin floating

PGood (Pin8): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider. The value of the pull-up resistor determines the current in the open-drain NMOS when the converter is not regulating, which should be limited to 50uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) when the output voltage is outside a regulation window which is approximately ±6.5% around the selected Vout (this occurs for large transient variations on Vout, in disable mode, during a restart, and in case the under-voltage, over-temperature or over-current protections are triggered).

Enable (Pin 9): Enable input. bPOL2V5_V3.3 is normally disabled and requires a voltage above 840 mV (typical value) applied to this pin to be enabled and start it switching operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 2.5V. There is an hysteresis, to switch off bPOL2V5_V3.3 the Enable pin must be lower than 400mV (typical value). The polarity of the pin can be inverted by connecting INV_Enable (Pin7) to ground, in which case bPOL2V5_V3.3 is enabled for applied voltages below 840mV. Note that an embedded 1 MΩ resistor pulls the voltage of the Enable pin to ground.

R_freq (Pin 12): Frequency Selector. A resistor placed between this Pin and the board ground determines the switching frequency of the converter. The frequency must be in the 3 – 4.5 MHz range. The default 70 kΩ resistor leads to a switching frequency of 4 MHz

(typical value), and this resistance value must be used when possible.

Gnd_control (Pin 13-20, 22-30, 32-40): Ground of the control electronics of the converter. It must be connected to the PCB ground plane.

R_OCP_neg (Pin 21): Negative over-current protection limit selector. A resistor placed between the R_OCP_neg pin and the board ground determines the limit of the negative overcurrent.
Concerning the negative over-current limit, the default resistance of 5.6 kΩ triggers the protection for an instantaneous inductor current of about OCP_neg=-2.35 A: the corresponding load current $Iout_{OCP}$ at which the protection is triggered can be estimated as:

$$Iout_{OCPneg} = OCP\_neg + (Vin-Vout)(Vout/Vin)/(2Lf_{sw}),$$

where L is the inductor value and f_{sw} is the switching frequency. $I_{out,OCP}$ is thus around -1.55 A with Vin = 2.5 V, Vout = 1.2 V, f_{sw} = 4 MHz and L= 100 nH.

Phase (Pin 41-49, 51-59, 111-119, 122-124): to be connected to the 100 nH inductor. A toroidal inductor is preferable for integration in High-Energy Physics detectors, in order to reduce the emission of electromagnetic noise. If a solenoid is chosen, the shield should be at a distance of at least 5 mm from the inductor to avoid a large decrease in the inductance value. Measurements are needed to quantify the reduction of the inductance due to the shield, in order to ensure that it is larger than 80 nH.

Vin_control (Pin 50, 60): Input Voltage for the control electronics of the converter. It is recommended to connect it to Vin close to the input capacitors (2x 2.2 µF). To guarantee a clean power supply voltage for the control circuitry, an additional 100 nF capacitor must be placed between Vin_control and ground, in close proximity to the ASIC.

Vin_power (Pin 61-80): Power Input Voltage. Input voltage of the power switches and drivers, where large current transients are flowing. Low-ESL input capacitors (2x TDK C0816X5R0J225M050AC are recommended) must be connected between this pin and GND_power as close to the ASIC as possible (see board design recommendations later on).

GND_power (Pin 81-110): Power Ground. This is the ground of the power train and drivers, where large current transients are flowing. All GND_power pins must be connected to the PCB ground plane by a large number of vias (ideally Via-in-Pad).

Vout (Pin 120): Regulated output voltage. This is an input pin connecting Vout to the control circuitry of the converter. It is internally connected to Pin 4 (Vout_Fb) to simplify the design of the board. It has to be connected to the two 10 µF output capacitors.

Trim_Enable (Pin 127): Enable trimmed reference voltage. E-fuses are included on chip to allow the trimming of the reference voltage. The reference voltage of bPOL2V5_V3.3 is trimmed to 300 mV ± 1 mV during production tests. If the Trim_Enable pin is left floating, the e-fuses determine the value of the reference voltage (the pin is connected to a 1.2 V internal rail through a 250 kΩ pull-up resistor). If Trim_Enable is connected to ground, the e-fuses are ignored, and the reference voltage assumes a default value. This functionality can be useful in case a malfunctioning of the e-fuses occurs.

PTAT (Pin 128): Proportional To Absolute Temperature. This pin provides a voltage which is proportional to the on-chip temperature, with a slope of about 4 mV/ºC. This pin can provide up to 7 µA of current.

Not connected pins NC (Pin 5-6-31-125-126-129): to be left floating. These are test pins that should not be used.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage – Vin_power, Vin_control	2.1	2.5	V
Output voltage – Vout	0.6	1.5	V
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	3	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	4.5	W
Switching frequency	3	4.5	MHz
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	ºC
Inductor value	80	120	nH
Enable voltage		2.5	V
Power Good voltage		2.5	V

Electrical Specifications

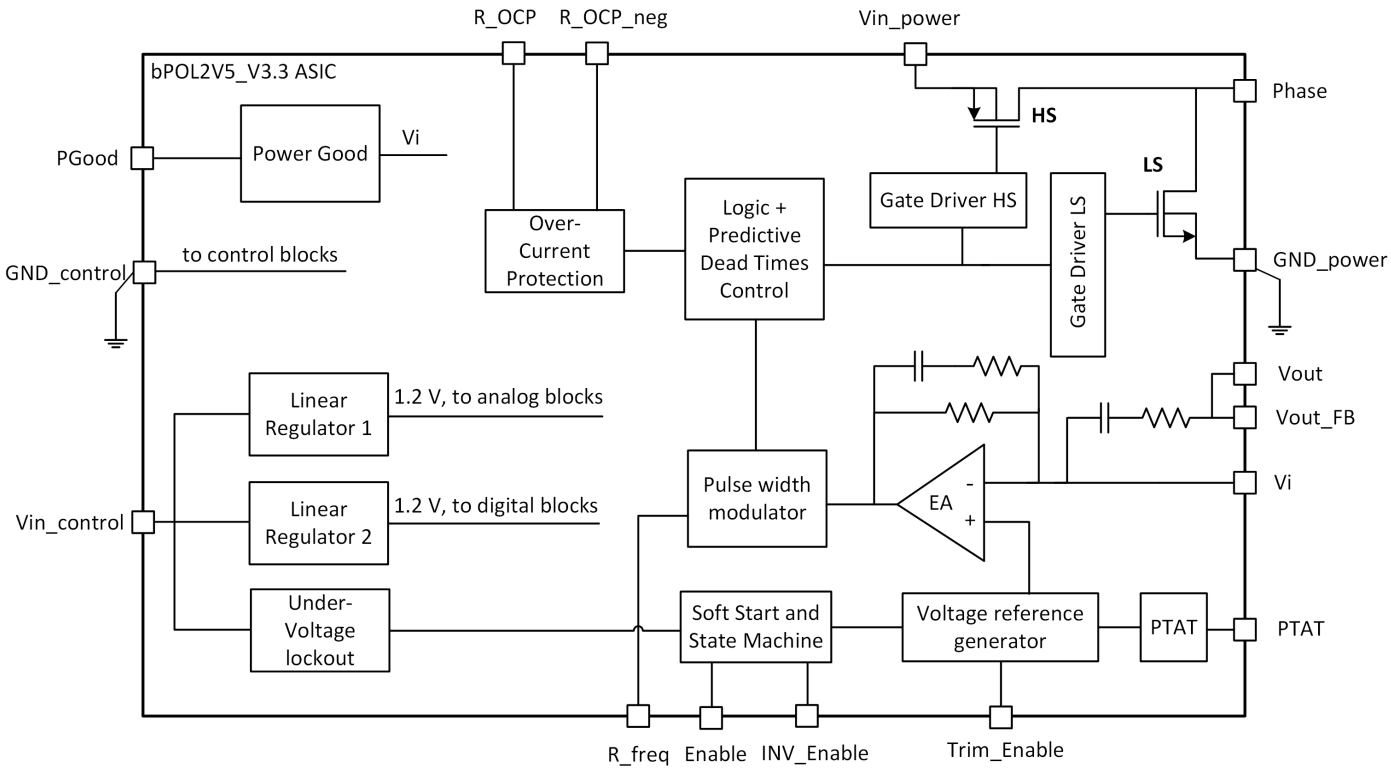
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
Vin_power, Vi_control	Input voltage supply range	Converter operational	2.1	-	2.5	V
Iin	Input current for control electronics (via Vin pin)	En pin low, converter disabled	-	6.5	-	mA
PWM						
DMax	Maximum Duty Cycle		-	99	-	%
DMin	Minimum Duty Cycle		-	0	-	%
Error Amplifier						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	50	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	20	-	V/µs
Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note1)*	1.85	1.97	2.05	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note1)*	1.7	1.81	1.95	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note1)*	-	840	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note1)*	-	400	-	mV
Protections						
OCP_pos	Positive Over-Current Protection level (instantaneous inductor current)	Vin = 2.5 V, Vout = 1.2 V, f_{sw} = 4 MHz, L = 100 nH, Tcoolingpad ≈ 18ºC *(note2)*	-	4.7	-	A
OCP_neg	Negative Over-Current Protection level (instantaneous inductor current)	Vin = 2.5 V, Vout = 1.2 V, f_{sw} = 4 MHz, L = 100 nH, Tcoolingpad ≈ 18ºC	-	-2.35	-	A
OTPStartTh	Over Temperature Protection start threshold	Converter on with zero load (to minimize self-heating) *(note3)*	94	104	133	ºC
OTPStopTh	Over Temperature Protection stop threshold	Converter on with zero load (to minimize self-heating) *(note3)*	59	70	94	ºC
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=2.5V, Vout=1.2V, f=4MHz, L=100nH, Tcoolingpad≈18ºC, *(note2, note4)*	300	500	770	us
Power Good						
OV	Output Over Voltage PGood upper threshold		-	+6.5	-	%
UV	Output Under Voltage PGood lower threshold		-	-6.5	-	%
Proportional To Absolute Temperature signal						
PTAT	Analog output voltage	Converter disabled, environmental T sweep	-	4	-	mV/ºC

Notes

Note 1: Values obtained by measuring 16 samples of bPOL2V5_V3.3 at room temperature.

Note 2: Values obtained by measuring 22 samples of bPOL2V5_V3.3 at room temperature.
Note 3: Average values obtained by measuring 8 samples of bPOL2V5_V3.3.
Note 4: The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

Block Diagram



Operation

bPOL2V5_V3.3 is a buck DCDC converter working in continuous conduction mode, which has been designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace. The typical application at steady large load current implies very relaxed requirements on quiescent current, while a fast feedback loop is at premium for some detectors where current consumption might have an instantaneous threefold increase.

Output voltage selection
The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and ground (Figure 1). The reference voltage for the Error Amplifier of bPOL2V5_V3.3 is trimmed to 300 mV ± 1 mV during production tests using e-fuses.

Switching frequency
The switching frequency of the converter can be adjusted with one external resistor, which provides the bias current to the embedded oscillator. The frequency range is 3 – 4.5 MHz. At lower frequency, the peak-to-peak current in the 100 nH air-core inductor increases and determines higher conduction losses and an earlier onset of the Over-Current Protection. At higher frequency, switching and driving losses increase.

Embedded linear regulators
While it can operate from a supply voltage of up to 2.5 V, the control electronics in bPOL2V5_V3.3 requires powering at 1.2 V. Two linear regulators are embedded to provide the appropriate voltage to the analog and to the digital control circuitry. All storage capacitors required for the regulators are on-chip and have been sized to ensure steady voltage even during large current surges.

Under-Voltage lockout
The embedded linear regulators need a sufficient level of over-voltage to provide a stable 1.2 V supply to the control circuitry, while a minimum value of Vin must be reached to guarantee proper operation of the gate drivers. To prevent faulty operation, an on-chip comparator only enables the converter when the input voltage rises above 1.97 V (typical value). A hysteretic operation of the comparator leads to a disabling of bPOL2V5_V3.3 when Vin drops below 1.81 V (typical value).

Enabling bPOL2V5
If the INV_Enable pin is left floating (as recommended), the circuit will not start operating when a sufficient Vin is applied to its input unless the Enable pin has been asserted by applying a voltage above 840 mV (typical value). Once the converter is on, the implemented hysteresis on the Enable pin is such that the converter is turned off applying a voltage below 400 mV (typical value) on Enable. bPOL2V5_V3.3 can hence be turned on-off by a control signal without the need of removing the power to its Vin bus, which allows an easy parallelization on the same supply bus (each bPOL2V5_V3.3 providing regulated power to a different load).
If the INV_Enable pin is connected to ground, the polarity of the Enable pin is reversed. Therefore, the Enable pin must be asserted by applying a voltage above 840 mV (typical value) to disable the converter. Once it is disabled, Enable must be lowered below 400 mV (typical value) to enable bPOL2V5_V3.3.

Soft Start procedure
When the converter is enabled, a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the error amplifier (EA), the output voltage reaching the nominal value in few hundreds of µs (there are significant sample-to-sample variations of the ramp duration, which in the measured samples ranged between 300µs and 770µs). Every time the converter is disabled – either by acting on the Enable pin, by under-voltage lockout, or by over-temperature detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the four states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference of the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PGood output pin is used to signal that bPOL2V5_V3.3 is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 2.5V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is in the 'on' state otherwise: in disabled state (Enable pin low), in an over-temperature condition and when the output voltage is outside a ±6.5% window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PGood to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 50uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PGood pin is 2.5V.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip temperature and disables bPOL2V5_V3.3 when it reaches about 105ºC. The OTP has a hysteresis of about 30ºC, hence the converter restarts (with a Soft Start) when the junction temperature decreases below about 70ºC. A significant sample-to-sample variation of the OTP temperature thresholds has been found in measurements (see the Electrical Specifications table above).

Over-Current Protection (OCP)
The positive and negative OCP employ peak detectors, respectively operating on the current flowing in the high-side (HS) and in the low-side (LS) switches. They are used to guarantee the reliable operation of the converter in the presence of faulty loads or when large and fast load transients occur.
The peak current that triggers the positive OCP protection can be tuned by means of the resistor connected between the R_OCP pin and ground.
Using the default 12.4 kΩ resistor, the positive OCP is activated when the current in HS exceeds about 4.7 A. When this occurs, HS is immediately turned off. If the excessive load current condition persists, the on-time of HS is not determined anymore by the feedback loop (which would require longer on-times to provide more output power) but by the OCP, and therefore the output voltage drops. In these conditions, also the switching frequency

decreases. If the output voltage drop exceeds 6.5% of the nominal value of Vout, PGood is pulled to ground. The peak current of 4.7 A translates into a different load current depending on the input and output voltage, on the switching frequency and on the inductor value, as presented above (see description of the R_OCP pin).
The negative peak detector detects large negative currents inside the low-side transistor LS, which may be generated when a large and fast transient occurs on Vin or on the load. The current value that triggers the negative OCP protections can be tuned by means of the resistor connected between the R_OCP_neg pin and ground.
Using the default 5.6 kΩ resistor connected to the R_OCP pin, the negative OCP is triggered when the instantaneous current is lower than about -2.35 A. When this occurs, the speed of the gate drivers of the low-side switch is decreased to avoid large over-voltages at the switching instants.
To guarantee the correct operation of the converter in all conditions, it is strongly recommended to use the default value of the resistors connected to R_OCP and to R_OCP_neg.

Compensation network
The compensation network is fully integrated and determines a typical loop bandwidth of about 190 kHz in the recommended operation conditions (in terms of switching frequency, input and output voltage, inductor value and on-board passives). bPOL2V5_V3.3 is hence capable of quickly adjusting the output voltage in case of output load transients.

Proportional To Absolute Temperature (PTAT) voltage
The PTAT analog signal can be used to monitor the on-chip temperature of the bPOL2V5_V3.3 ASIC during operation. The absolute value of the PTAT voltage at a given T has a wide sample-to-sample variability (up to 200 mV). However, the PTAT increase with respect to T shows a linear behavior with slope 4 mV/ºC. This has been verified on 6 pre-rad samples and on 3 samples irradiated with X-rays, and the measurement results are shown in Figure 2.
The PTAT pin can provide up to 7 µA of current.

Cooling
bPOL2V5_V3.3 is specified for operation up to 4.5 W output power. With an efficiency of 80 % in case of large load current and not–cryogenic cooling, this translates in 0.9 W lost in the converter. Most of this power is dissipated by the bPOL2V5_V3.3 ASIC and needs to be transferred to the cooling system efficiently. Bump bonding limits heat transfer, therefore it is strongly suggested to use the via-in-pad technique to ensure a good contact of the bPOL2V5_V3.3 ground pins to the ground plane of the PCB, which itself must have a good thermal contact to the cooling system.

Radiation tolerance
The full development of bPOL2V5_V3.3 has been driven by the radiation tolerance goal of reliable flawless operation in the HEP experiments at the CERN High Luminosity Large Hadron Collider (LHC).
X-ray irradiations have highlighted that bPOL2V5_V3.3 is capable of continuous operation up to 100Mrad (SiO2) of Total Ionizing Dose.
Concerning Single Event Effects (SEE), bPOL2V5_V3.3 has been irradiated with heavy ions up to a Linear Energy Transfer (LET) of 40MeVcm2/mg, showing no destructive SEEs or output power interruptions. On a pre-rad sample, no transients exceeding ±5% on the output voltage have been detected up to LET=40MeVcm2/mg. On a sample previously irradiated up to 100Mrad (SiO2), no transients exceeding ±10% on the output voltage have been found up to LET=28MeVcm2/mg, while for LET=40MeVcm2/mg 8 transients below -10% have been found for a total fluence of 1e6 ions/cm2. Figure 17 shows an example of such transients.
Concerning displacement damage, a neutron irradiation has highlighted that bPOL2V5_V3.3 is tolerant up to a total fluence of 2e16 n/cm2. The efficiency after irradiation is depicted in Figure 15. Irradiation with a 24 GeV/c proton beam demonstrated that bPOL2V5_V3.3 is tolerant to a total fluence of 6.1e15 p/cm2, and the related efficiency curves are presented in Figure 16.

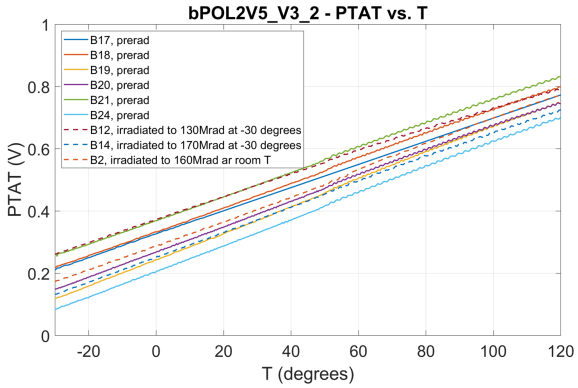


Figure 2: Measured PTAT voltage of bPOL2V5_V3.2 (previous prototype, where the PTAT circuit is identical to bPOL2V5_V3.3) vs. temperature for pre-rad samples (solid lines) and for samples irradiated with X-rays (dashed lines).

Measured performance – pre-rad

The efficiencies and the regulation performance presented in the following have been obtained by measuring Vout in correspondence of the 2x10 µF output capacitors (placed in close proximity to the ASIC), and by measuring Vin in correspondence of the 2x2.2 µF input capacitors (placed in close proximity to the ASIC). All the measurements have been carried out using L=100 nH and a switching frequency of 4 MHz.

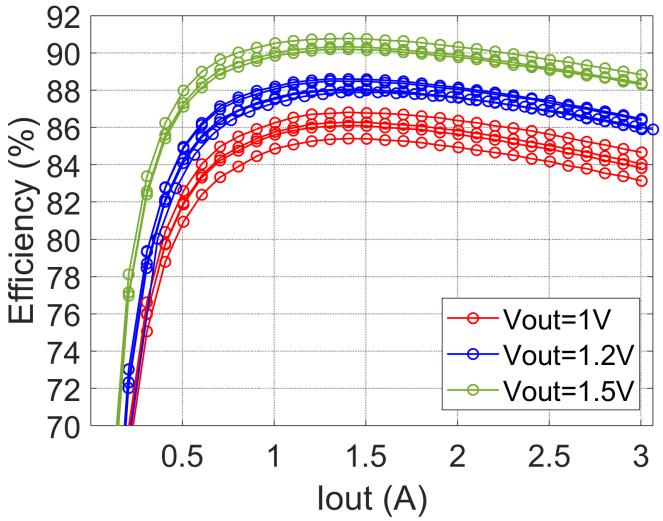


Figure 3: Efficiency for Vin=2.5V and different load currents at room temperature (with the module in good thermal contact with a cooling plate at about 18°C). Each line corresponds to a different sample of bPOL2V5_V3.3

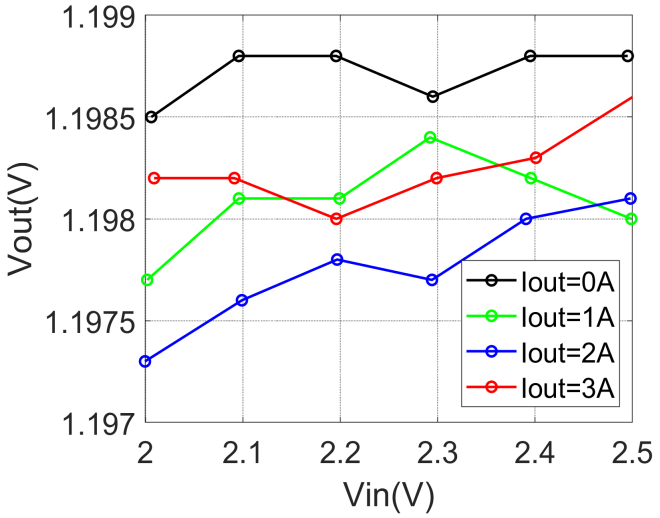


Figure 4: Line and load regulation of a sample of bPOL2V5_V3.3 for Vin=2.5V, at room temperature (with the module in good thermal contact with a cooling plate at about 18°C).

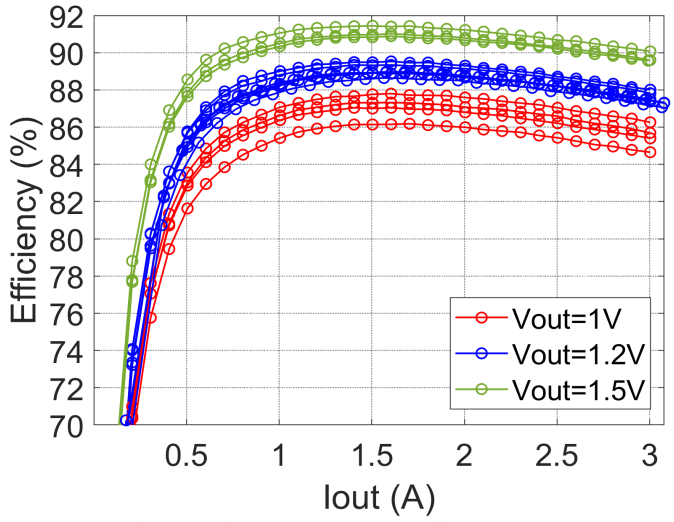


Figure 3: Efficiency for Vin=2.5V and different load currents at -30°C (-30°C ambient temperature, and module in good thermal contact with a cooling plate at -30°C). Each line corresponds to a different sample of bPOL2V5_V3.3.

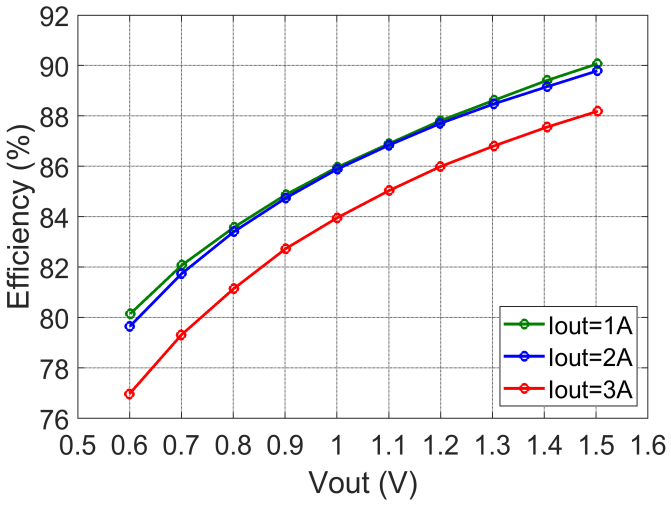


Figure 5: Efficiency vs. Vout for Vin=2.5V for different loads at room temperature, as measured on a sample of bPOL2V5_V3.2 (previous prototype having the same efficiency).

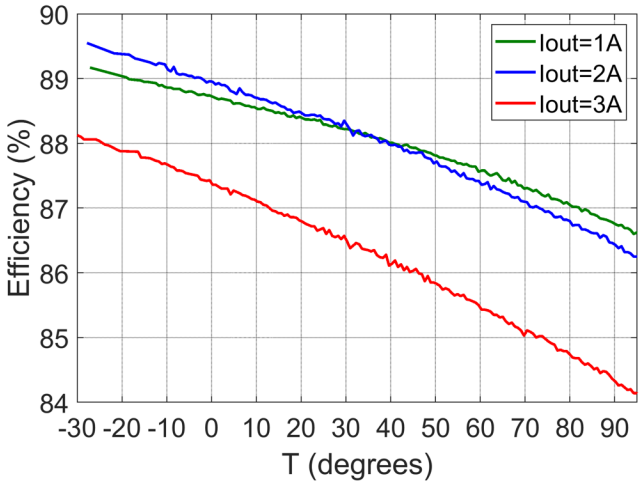


Figure 6: Efficiency vs. temperature for Vin=2.5V and Vout=1.2 V for different loads, as measured on a sample of bPOL2V5_V3.2 (previous prototype having the same efficiency).

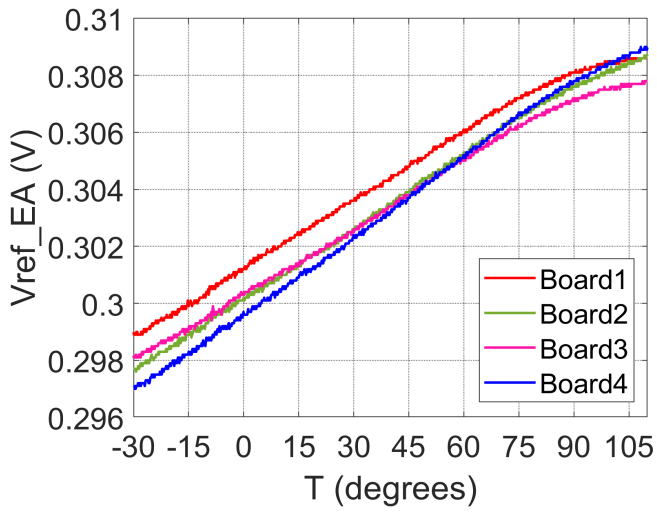


Figure 7: Reference voltage variation vs. temperature, as measured on 4 samples of bPOL2V5_V3.3. The measurement was performed on untrimmed samples. Since Vout is proportional to the reference voltage, an increase of Vout in temperature is found.

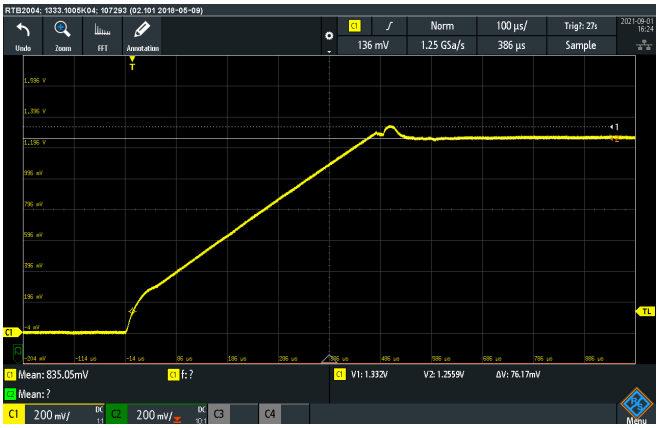


Figure 8: Output voltage measured on a sample of bPOL2V5_V3.3 at room temperature during the Soft Start, for Vin=2.5 V, Vout=1.2 V, Iout=0 A. The small overshoot on Vout at the end of the Soft Start is inherent to the operation of the controller.

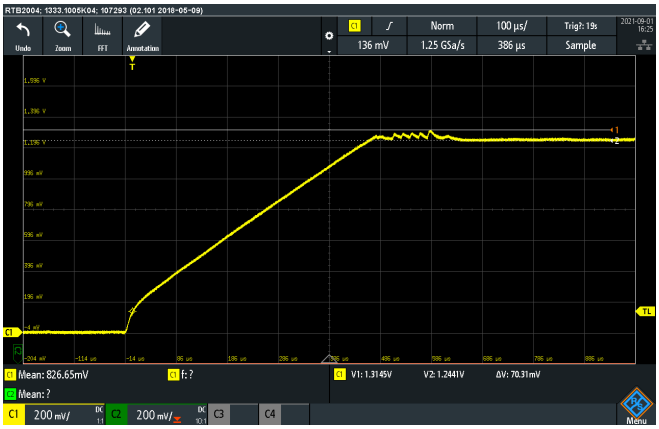


Figure 9: Output voltage measured on a sample of bPOL2V5_V3.3 at room temperature during the Soft Start, for Vin=2.5 V, Vout=1.2 V, Iout=2.1 A. The small overshoots on Vout at the end of the Soft Start are inherent to the operation of the controller.

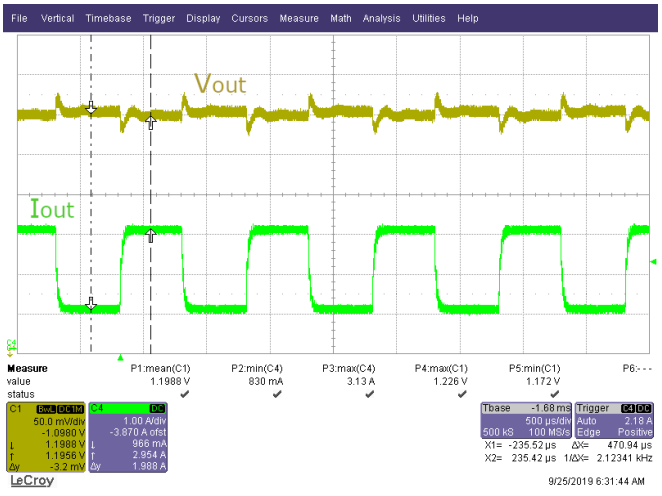


Figure 10: Output voltage measured on a sample of bPOL2V5_V3.2 (previous prototype with the same dynamic characteristics as bPOL2V5_V3.3) when transient variations in its load from 1 to 3 A are applied, for Vin=2.5 V and Vout=1.2 V. The rise and fall times of the load are 25 µs.

Measured performance – irradiations

X-ray irradiations of bPOL2V5_V3.3 have highlighted that the performance degradation induced by Total Ionizing Dose is larger for higher dose rates. The presented efficiency degradation is therefore expected to be significantly larger than the one that will be found in any real application of the converter (where the dose rate will be lower).

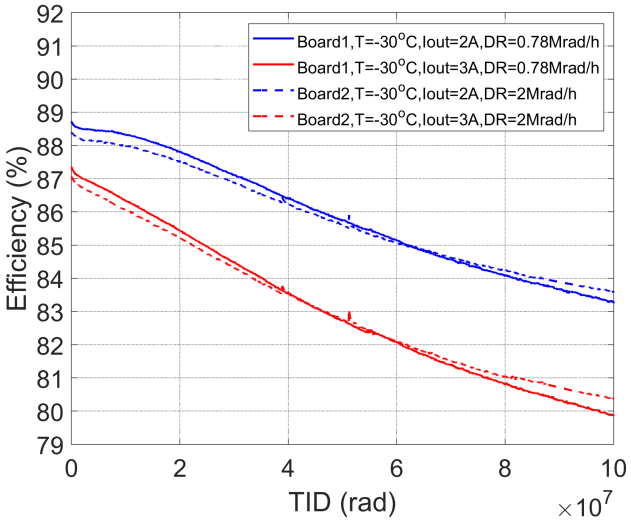


Figure 11: Evolution of the efficiency of 2 samples of bPOL2V5_V3.3 during X-ray irradiations (Vin=2.5 V, Vout=1.2 V, T=-30°C). The dose is referred to SiO_2.

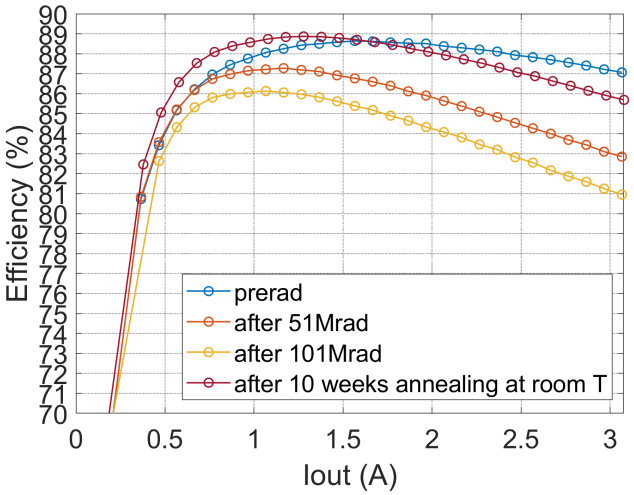


Figure 12: Efficiency vs. load current for a sample of bPOL2V5_V3.3 before, during and 10 weeks after the X-ray irradiation (Vin=2.5 V, Vout=1.2 V, T=-30°C). The dose is referred to SiO_2. A significant recovery of the converter performance has been found after the annealing.

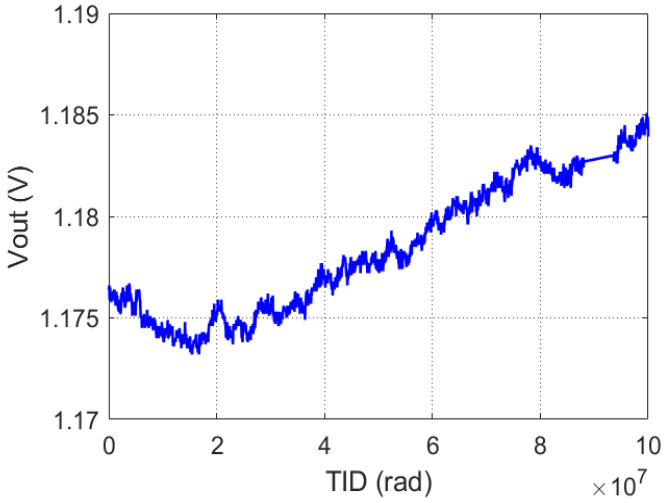


Figure 13: Vout of a sample of bPOL2V5_V3.3 during an X-ray irradiation with a dose rate of 0.78 Mrad/h (Vin=2.5 V, T=-30°C). The dose is referred to SiO_2. During the annealing, the value of Vout does not significantly change.

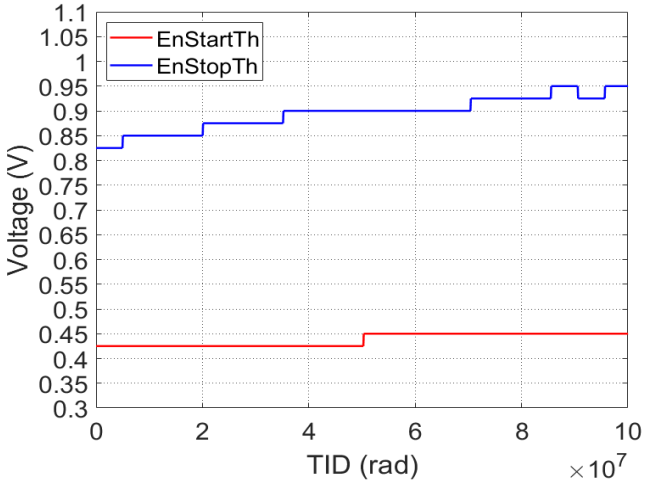


Figure 14: Evolution of the Enable pin thresholds with TID (T=-30 °C, dose rate 2.8Mrad/h). The dose is referred to SiO_2.

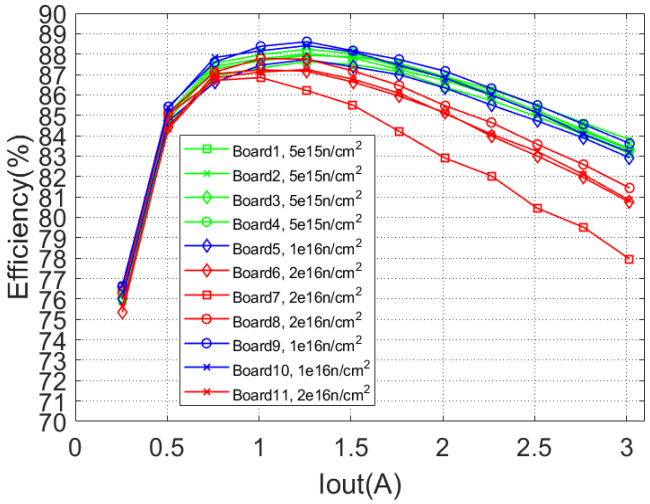


Figure 15: Efficiency after neutron irradiation of 11 samples of bPOL2V5_V3.3 irradiated to different total fluences. Vin=2.5V, Vout=1.2V, room temperature.

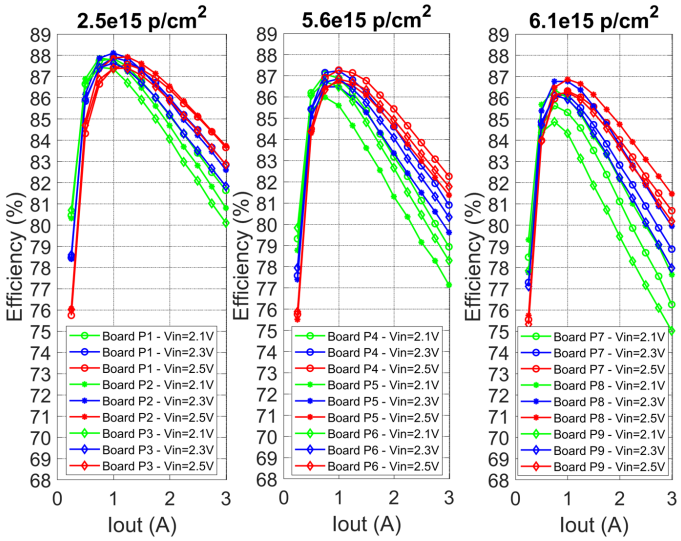


Figure 16: Efficiency after proton irradiation (with a 24 GeV/c proton beam) of 9 samples of bPOL2V5_V3.3, Vout=1.2V, room temperature.

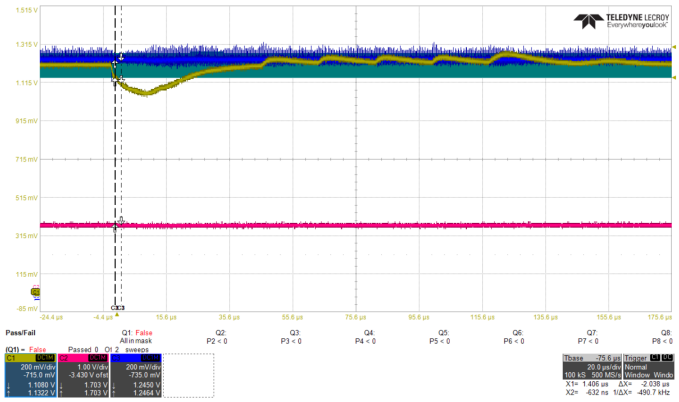


Figure 17: Example of a negative transient found on the output voltage of a sample of bPOL2V5_V3.3 (yellow trace) previously irradiated to 100 Mrad, for a heavy ion irradiation and Linear Energy Transfer = 40 MeVcm²/mg.

Board Layout Considerations

Over-voltages are experienced by the on-chip devices during the switching operation of the converter, due to the dI/dt on the parasitic input inductors. Due to the radiation tolerance requirements, the voltage rating of the used devices (3.3 V) is close to the maximum input voltage (2.5 V). Therefore, the over-voltages must be mandatorily minimized to guarantee a reliable operation.
This motivates the choice of a flip-chip assembly, which minimizes the bonding parasitic inductance compared to wire-bonding.
A study has been carried out to optimize the PCB to achieve minimal input parasitic inductance. The resulting board design uses the via-in-pad technique for the ground connections, and a similar layer stack and placement of the components must be adopted for all designs using bPOL2V5_V3.3. More information is available contacting Giacomo.Ripamonti@cern.cn or Stefano.Michelis@cern.ch.
The ESL of the input capacitors Cin also contributes to the total input parasitic inductance. Thus, low-ESL capacitors must be used (2x2.2 µF, see Figure 15, TDK C0816X5R0J225M050AC capacitors have been adopted in the optimized layout). In addition, they must be placed as close as possible to the Vin_power and GND_power pins, as shown in Figure 16.
An additional 100 nF capacitor Cin,ctrl must be placed as shown in Figure 16 to guarantee a clean power supply voltage for the control circuitry.
It is recommended to use 2x10 µF for the output capacitance Cout. If an additional LC filter is needed at the output (see Figure 15), the values of its passive components must be Loutf = 2.5 nH and Coutf = 22 µF to achieve output ripple filtering and a stable operation of the converter.
An input LC filter is necessary to avoid the injection of disturbances at the switching frequency or at its harmonics into the power supply, and to suppress the noise from the power supply. The default values of its components Linf and Cinf are respectively 12 nH and 22 µF (see Figure 15).
In order to guarantee a reliable operation, each PCB design using bPOL2V5_V3.3 must be validated by extracting the input parasitic inductance and by comparing it to the value obtained for the optimized PCB.

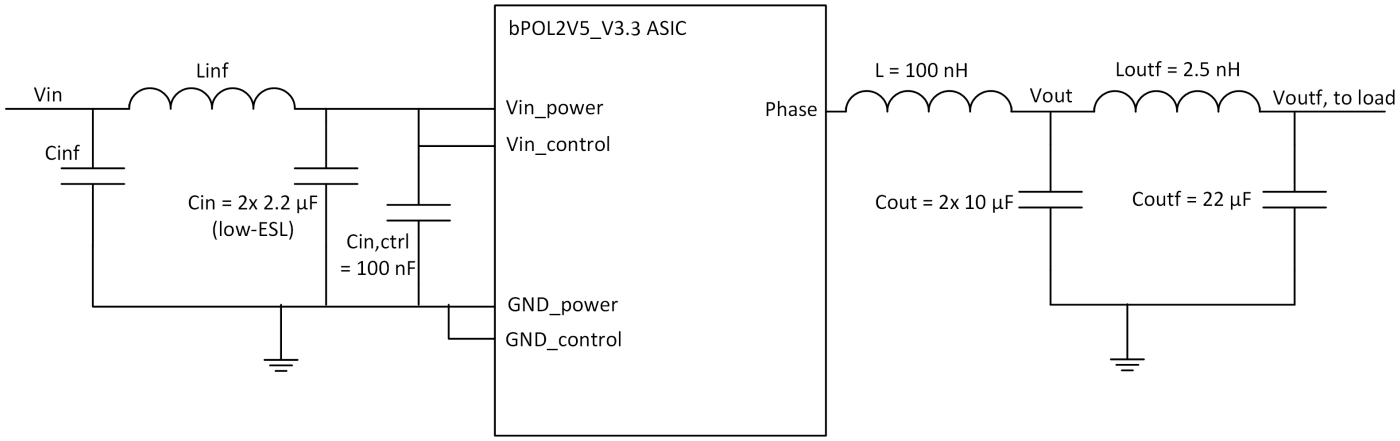


Figure 15: Schematic of bPOL2V5_V3.3, using additional input and output LC filters.

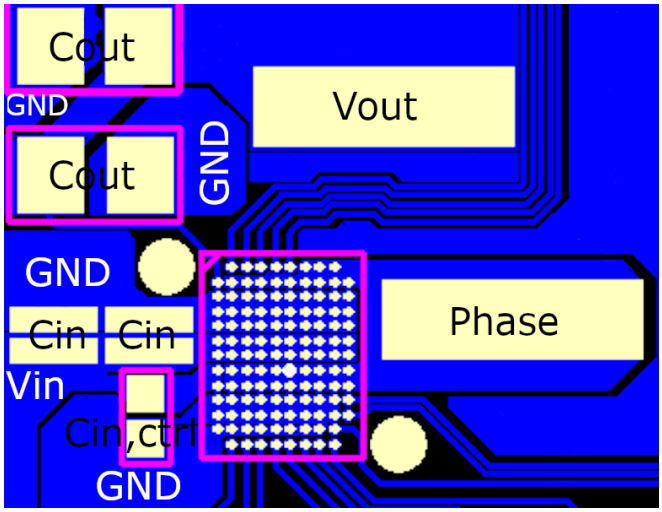


Figure 16: Top layer of the optimized PCB layout for bPOL2V5_V3.3.

Bumping description

bPOL2V5_V3.3 is a bump bonded ASIC with 125 pads. Chip dimension is 3.1 x 4 mm, UBM has a diameter of 110 µm with polyamide as top passivation layer.
SnAg bumps are deposited by the foundry with a pitch of 300 µm, height 100 µm and diameter 132 µm.
The four pads on the corner are missing due to foundry design rules. An extra pad has been removed from the top left corner to allow easier orientation for mounting on PCB.

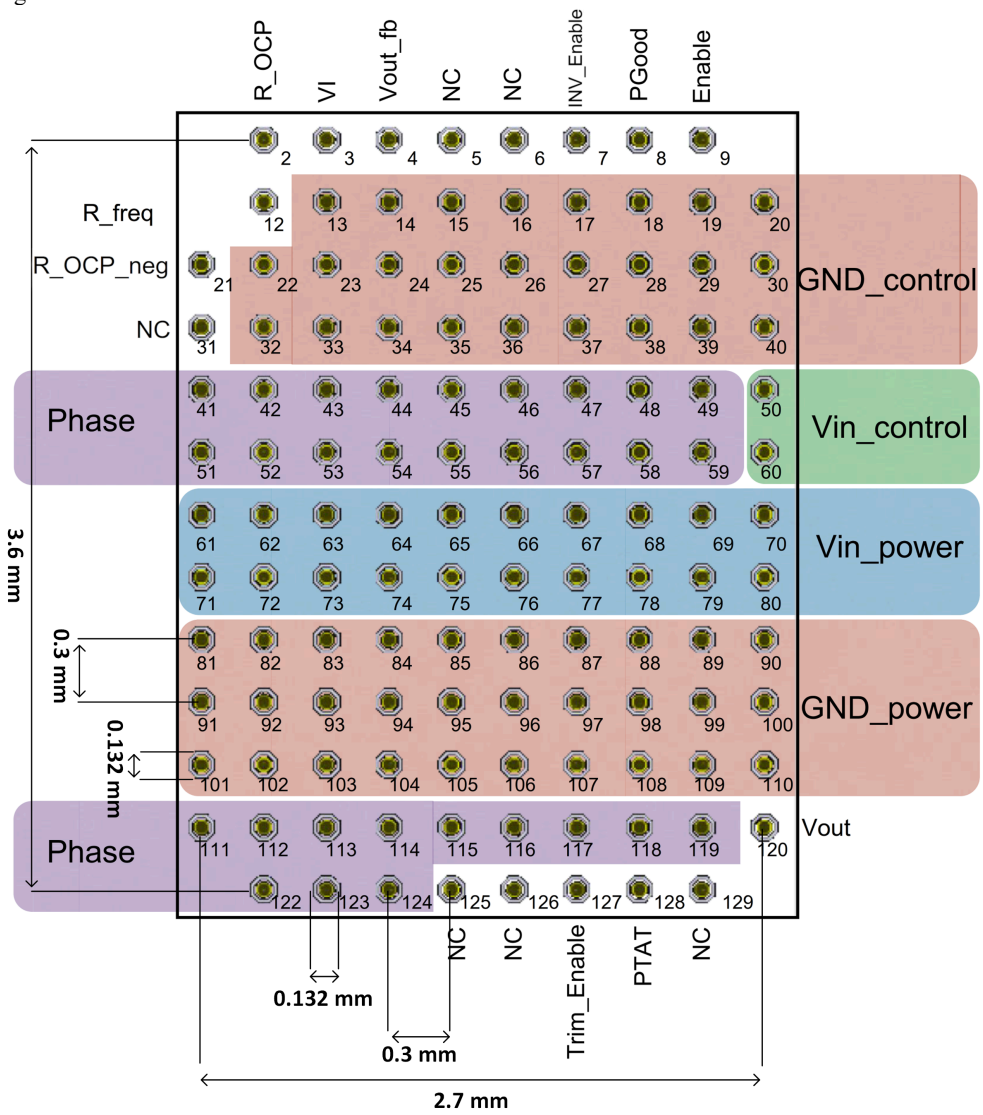


Figure 17: bPOL2V5_V3.3 pin layout (recommended land pattern on the PCB).

Revision history

Revision	Date	Description
1.0	September2021	First release of the document
2.0	February2022	Update after measurements on samples with trimmed reference voltage
3.0	March2022	Update with measurements on proton-irradiated samples