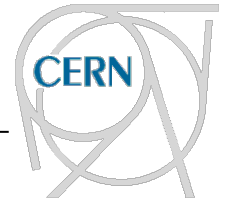


# bPOL2V5\_V2.2



## Radiation tolerant 3.6W Synchronous Step-Down Buck DC/DC converter

### Features

- Input voltage range 2 to 2.5V
- Continuous 3A load capability
- Integrated N and P-channel MOSFETs
- Adjustable switching frequency 2-10MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (200KHz) for good transient performance
- Over-Current protection
- Under-voltage lockup
- Power Good output
- Enable Input
- Radiation tolerant: The previous prototype (DCDC2S) has been tested for TID up to 200Mrad(Si), continuous operation during exposure to heavy ions of LET up to 64MeVcm<sup>2</sup>mg<sup>-1</sup> with short transients below 20% of the nominal Vout (no destructive event, no output power interruption).

### Applications

Second stage Point Of Load in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

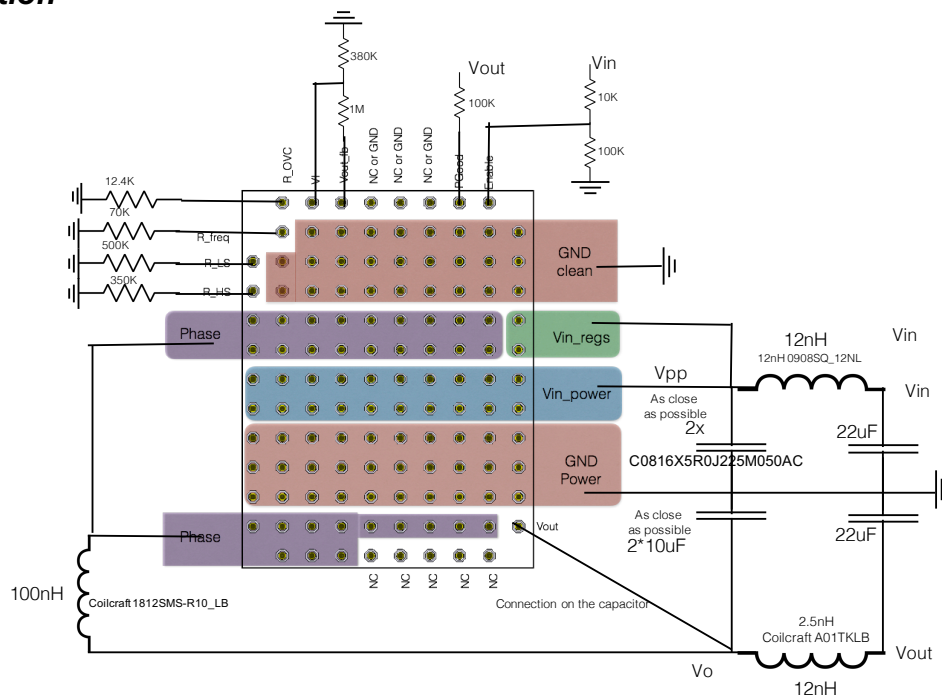
### Description

bPOL2V5\_V2.2 is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of

power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the previous prototype (DCDC2S) converter capable of continuous operation up to more than 200Mrad(Si) total ionizing dose. Displacement damage tests have to be performed. Single Event Effects resilience has been built-in, and the circuit has been tested free of destructive SEEs and of output power interruptions during irradiations with heavy ions up to an equivalent LET of 64MeVcm<sup>2</sup>mg<sup>-1</sup> (at 60° incidence; no data available for higher LETs). bPOL2V5\_V2.2 has been designed for operation in a strong magnetic field in excess of 40,000 Gauss, and has been optimized for air-core inductors of 40-100nH: to be compatible with these small coil values, its switching operation is in the 4-10MHz range (4MHz for maximum efficiency).

The monolithic construction of bPOL2V5\_V2.2, with the integration of the power train, makes the converter a space-efficient solution to provide a second stage POL regulation from a 2.5V supply rail. Its protection features include Over-Current and Input Under-Voltage to improve system-level security in the event of fault conditions.

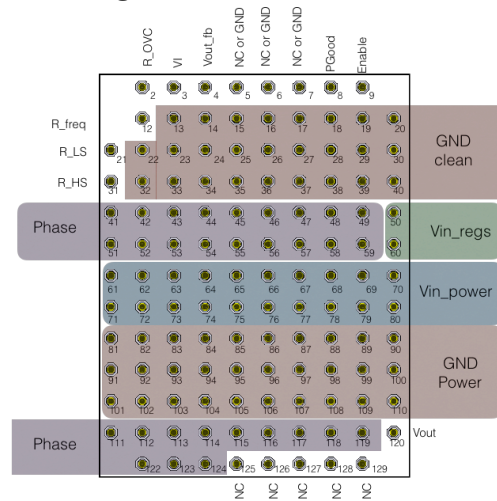
### Typical application



## Absolute Maximum Ratings

Power Input Voltage Vin_Power.....	-0.3V to +2.5V
Control Input Voltage Vin_regs.....	-0.3V to +2.5V
Phase Voltage.....	-0.3 V to Vin (DC), -1 to 2.5 V (AC, 10ns)
Feedback input Voltage of the E/A Vi.....	-0.3V to +2.5V
Frequency selector Rf.....	-0.3V to +2.5V
Power transistor size toggle HalfSw.....	-0.3V to +2.5V
Reference voltage toggle Ref1V2.....	-0.3V to +2.5V
Converter Enable En .....	-0.3V to +2.5V
Power good PGood.....	-0.3V to +2.5V
Output Voltage Vout.....	-0.3V to +2.5V
Current in PGood pin (when PGood is negated).....	50uA

## Pin Configuration



## Pin Function

**R\_OVC (Pin 2):** Over-current limit Selector. A resistor placed between this Pin and the board GND determines limit of the overcurrent. A resistance of 12.7KOhm fixes the limit to 5A. This is the result of the simulation, to be confirmed with tests.

**Vi (Pin 3):** Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 200kHz, but the DC regulation voltage Vout is selected by the addition of 2 resistors building a voltage divider between Vout\_Fb and gnd. Vi is connected between the 2 resistors and the resulting voltage is compared to the internal reference voltage (about 0.3V). The resistor between Vout and Vi must have a value of 1MΩ, while the one between Vi and gnd is selectable (no resistor makes Vout = Vref). Vout and Vout\_Fb are internally connected. The positioning of the two is studied to allow easier integration on PCB, as Vout pin has to be connected as close as possible to the output capacitor and Vout\_Fb is sued to locate the resistor between Vout\_Fb and Vi.

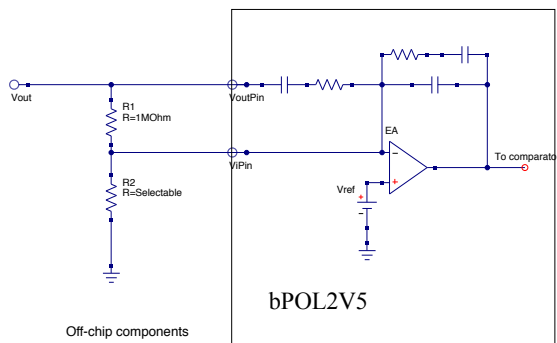


Figure 1: Configuring the output voltage.

**Vout\_Fb (Pin 4):** Regulated output voltage, internally connected with Vout pin. This is an input pin bringing the Vout back to the

converter’s feedback circuit. It must be connected as specified in the description of Pin 2 (Vi).

**Pin\_conf1-2 (Pin 5-7):** Configurable pin for testing purpose. To be defined if floating or connected to ground.

**PGood (Pin8):** Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 50uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout.

**En (Pin 9):** Enable input. bPOL2V5\_V2.2 is normally disabled and requires a voltage above 850mV applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V. Note that an embedded 1MΩ resistor pulls the voltage of the En pin to gnd.

**R\_freq (Pin 12):** Frequency Selector. A resistor placed between this Pin and the board GND determines the switching frequency of the converter. The recommended range for best performance is 4 MHz corresponding to a resistance of 70KOhm.

**Gnd (Pin 13-20, 22-30, 32-40):** Ground of the control electronics of the converter. It must be connected to the PCB ground plane.

**R\_LS (Pin 21):** Delay selector for Low Side turn on. A resistor of 500KOhm has to be connected towards ground.

**R\_HS (Pin 31):** Delay selector for High Side turn on. A resistor of 350KOhm has to be connected towards ground.

**Phase (Pin 41-49, 51-59, 111-119, 122-124):** to be connected to the 100nH inductor.

**Vin\_regs (Pin 50,60):** Input Voltage for the control electronics of the converter. It is recommended to connect it to Vin close to the input capacitor.

**Vin\_Power (Pin 61-80):** Power Input Voltage. Input voltage of the power switches and drivers, where large current transients are flowing. Low ESL input capacitances (recommended 2x C0816X5R0J225M050AC) must be connected between this pin and PGnd as close to the package as possible (see board design recommendations later on).

**GND\_Power (Pin 81-110):** Power Ground. This is the gnd of the power train and drivers, where large current transients are flowing. All PGnd pins must be connected to the PCB gnd plane by a large number of vias (ideally Via-in-Pad)

**Vout (Pin 120):** Regulated output voltage. This is an input pin bringing the Vout back to the converter's feedback circuit. It is internally connected to Pin 3 Vout\_Fb to simplify the design of the board. It has to connect to the output capacitor.

**Not connected pins NC (Pin 125-129):** to be left floating

## Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - PVin, Vin	2	2.5	V
Output voltage - Vout	0.6	1.5	V
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	3	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	4	W
Switching frequency	3.8	4.2	MHz
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	°C
Inductor value	80	120	nH
Enable voltage		2.5	V
Power Good voltage		2.5	V

## Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power</b>						
PVin, Vin	Input voltage supply range	Converter operational	2	-	2.5	V
Iin	Input current for control electronics (via Vin pin)	En pin low, converter disabled	-	3	-	mA
<b>PWM</b>						
DMax	Maximum Duty Cycle		-	100	-	%
DMin	Minimum Duty Cycle		-	0	-	%
<b>Error Amplifier</b>						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	50	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	20	-	V/μs
<b>Under-Voltage Lockout</b>						
VinStartTh	Vin start threshold	Vin rising trip level ( <i>note1</i> )	-	2	-	V
VinStopTh	Vin stop threshold	Vin falling trip level ( <i>note1</i> )	-	1.8	-	V
<b>Enable</b>						

EnStartTh	Enable start threshold	Enable rising trip level ( <i>note1</i> )	-	850	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level ( <i>note1</i> )	-	400	-	mV
<b>Protections</b>						
OCPpk	Over Current Protection peak level	Vin=2.5V, Vout=1.2V, f=4MHz, L=100nH, Tcoolingpad≈18°C, ( <i>note2</i> )	-	5	-	A
<b>Soft Start</b>						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=2.5V, Vout=1.2V, f=4MHz, L=100nH, Tcoolingpad≈18°C, ( <i>note1, note3</i> )		600		us
<b>Power Good</b>						
OV	Output Over Voltage PGood upper threshold			+6.5		%
UV	Output Under Voltage PGood lower threshold			-6.5		%

**Notes**

*Note 1:* Average value taken from measurements on previous prototype (DCDC2S).

*Note 2:* This value is an estimation from simulation

*Note 3:* The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

## Operation

bPOL2V5\_V2.2 is a DCDC converter designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace. The typical application at steady large load current with power provided from a remote supply (not from a battery) implies very relaxed requirements on quiescent current, while a fast feedback loop is at premium for some detectors where current consumption might have an instantaneous threefold increase.

### Output voltage selection

The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage to the Error Amplifier. This has been measured on previous prototype at around 300mV.

### Switching frequency

The switching frequency of the converter can be adjusted with one external resistor, which provides the bias current to the embedded oscillator. Although bPOL2V5\_V2.2 has been tested as functional over a wide range of frequency (4 to 10MHz), best performance is achieved with 4 MHz. At lower frequency, the peak-peak current in the small air-core inductor increases excessively and determines useless losses and possibly an early onset of the OCP. At higher frequency, driving losses increases dramatically and make the efficiency drop very sensibly.

### Embedded linear regulators

While it can operate from a supply voltage of up to 2.5V, the control electronics in bPOL2V5\_V2.2 requires powering at 1.2V. A number of linear regulators are embedded to provide appropriate voltage to the drivers of the power transistors, to the bandgap and reference current generator, to the analog and to the digital circuitry. All storage capacitors required for the regulators are on-chip and have been sized to ensure steady voltage even during large current surges.

### Under-Voltage lockout

The embedded linear regulators need a sufficient level of over-voltage to provide stable 1.2V voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above about 2V (on rising Vin). This comparator has an hysteresis and bPOL2V5\_V2.2 is disabled again when, for falling Vin, the input voltage drops below about 1.8V.

### Enabling bPOL2V5

The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has not been asserted by applying a voltage above about 850mV. bPOL2V5\_V2.2 can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each bPOL2V5\_V2.2 providing regulated power to a different load).

### Soft Start procedure

When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start

(SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the EA, the output voltage reaching the nominal value in about 600us in the nominal configuration using the 0.3V bandgap. Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

### Power Good flag

The PG output pin is used to signal that bPOL2V5\_V2.2 is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 2.5V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, in reset and when the output voltage is outside a  $\pm 6.5\%$  window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 50uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PG pin is 2.5V.

### Over-Current Protection (OCP)

OCP is integrated as a real peak detector on the current flowing during each cycle in the HS transistor. Current sensing takes place on the parasitic resistance of metal lines bringing the input current from the input pads to the HS transistor. When the instantaneous current exceeds about 6A (very approximate value), the PWM is reset and forces the HS to turn off. If the excessive load current condition persists, the on-time of the HS is not determined anymore by the feedback loop (which would require longer on-times to provide more output power) but by the OCP, and as a consequence the output voltage drops and a decrease of the switching frequency. This condition might endure as a steady state, PG being pulled to gnd if the output voltage drop exceeds 6.5% of the nominal. The peak current of 6A translates in different average output current depending on the input and output voltage, frequency and inductor value.

### Compensation network

The compensation network is fully integrated and determines a typical loop bandwidth of about 200kHz in the recommended operation environment (frequency, voltages, inductor, on-board passives). bPOL2V5\_V2.2 is hence capable of quickly adjusting the output voltage in case of output load transients.

### Cooling

bPOL2V5\_V2.2 is specified for operation up to 4W output power. With an efficiency of 80% in case of large load current and not-cryogenic cooling, this translates in 0.8W lost in the converter (including the resistance of the inductor and of other passive components). Most of this power is burnt by bPOL2V5\_V2.2 itself and needs to be transferred to the cooling system efficiently. The Bump Bonding is a limitation for heat transfer, therefore it is strongly suggested to use as much as via possible or via-in-pad

technique to ensure a good contact of bPOL2V5 ground pins to the ground plane of the PCB which itself must have a good thermal contact to the cooling system.

**Radiation tolerance**

The full development of bPOL2V5\_V2.2 has been driven by the radiation tolerance goal of reliable flawless operation in the HEP experiments at the CERN Large Hadron Collider (LHC). In particular, radiation tolerance specifications for applications in phase1 upgrades of the LHC include TID up to 20Mrad, displacement damage up to  $2.5 \times 10^{14}$  particles/cm<sup>2</sup> (1MeV n-equivalent), no destructive event (SEB, SEGR) and continuous supply of the correct output voltage in a hadron radiation environment (no SETs on the output beyond  $\pm 20\%$  of the nominal regulated voltage).

Radiation tolerance determined in the first place the choice of the CMOS technology used for the design: high-voltage transistors

were required not to be sensitive to SEB and SEGR during heavy ion tests up to an LET of  $30 \text{MeV} \cdot \text{mg}^{-1} \cdot \text{cm}^2$  (at normal incidence). For the control circuits, Hardness By Design (HBD) techniques have been systematically used to prevent the opening of leakage currents with TID. Results of SEE test campaigns at heavy ion and pulsed laser facilities enabled the measurement of the cross-section and the localization of weak points during the development, and were used to correct the final design.

Partial radiation characterization has been done on previous prototype (DCDC2S) up to more than 200Mrad and during exposure to heavy ions of LET up to  $64 \text{MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$  with short transients below 20% of the nominal Vout (no destructive event, no output power interruption).

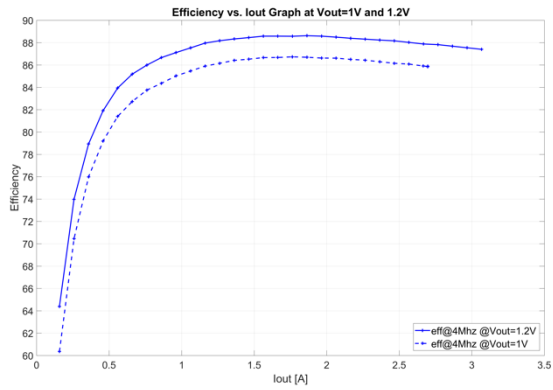


Figure 2: Efficiency for  $V_{out}=1V$  and  $V_{out}=1.2V$  and  $V_{in}=2.5V$  and different  $I_{out}$  with the module in good thermal contact with a cooling plate at about  $18C$ .

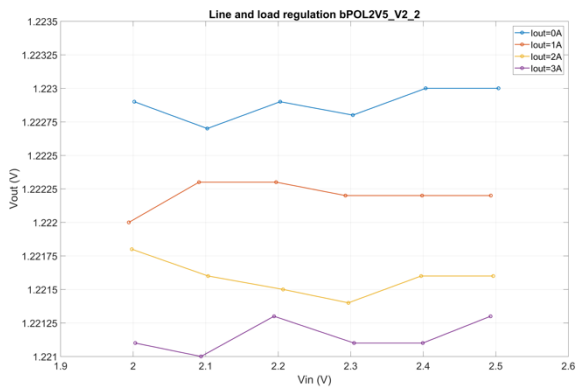


Figure 3: Line and load regulation with the module in good thermal contact with a cooling plate at about  $18oC$ .

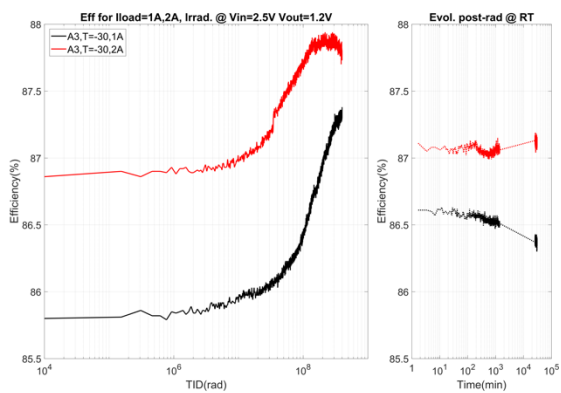


Figure 4: Efficiency variation with X-ray irradiation at  $-30C$ , for  $V_{in}=2.5V$ . Measurements are taken during irradiation step and during annealing at Room temperature. Last TID point is about  $400Mrad(SiO2)$ .

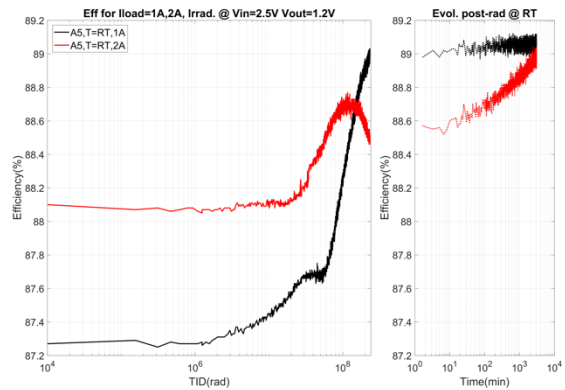


Figure 5: Efficiency variation with X-ray irradiation at  $25C$ , for  $V_{in}=2.5V$ . Measurements are taken during irradiation step and during annealing at Room temperature. Last TID point is about  $200Mrad(SiO2)$ .

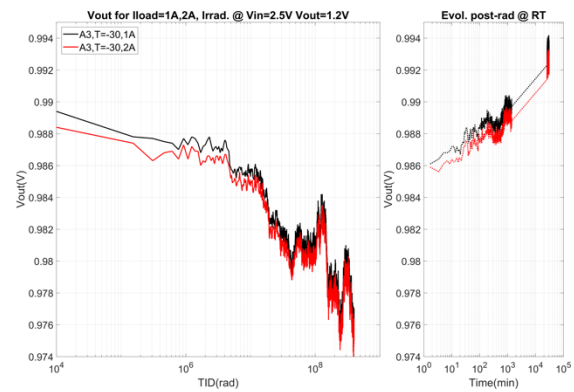


Figure 6:  $V_{out}$  variation with X-ray irradiation at  $-30C$ , for  $V_{in}=2.5V$ . Measurements are taken during irradiation step and during annealing at Room temperature. Last TID point is about  $400Mrad(SiO2)$ .

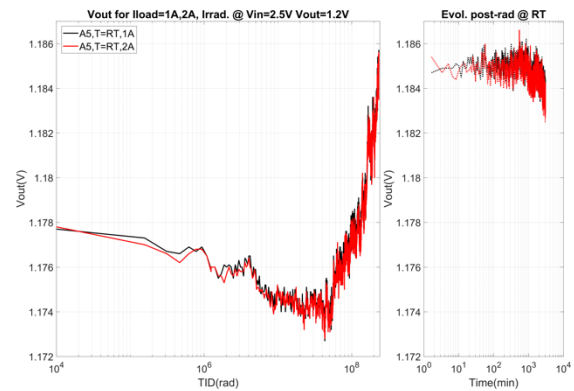


Figure 7: Efficiency variation with X-ray irradiation at  $25C$ , for  $V_{in}=2.5V$ . Measurements are taken during irradiation step and during annealing at Room temperature. Last TID point is about  $200Mrad(SiO2)$ .

### Bumping description

bPOL2V5\_V2.2 is a bump bonded ASIC with 125 pads. Chip dimension is 3x3.9mm, UBM has a diameter of 110um with polyamide as top passivation layer.

SnAg bumps are deposited by the foundry with a pitch of 300um, height 100um and diameter 132um.

The four pads on the corner are missing due to foundry design rules. An extra pad has been removed from the top left corner to allow easier orientation for mounting on PCB.

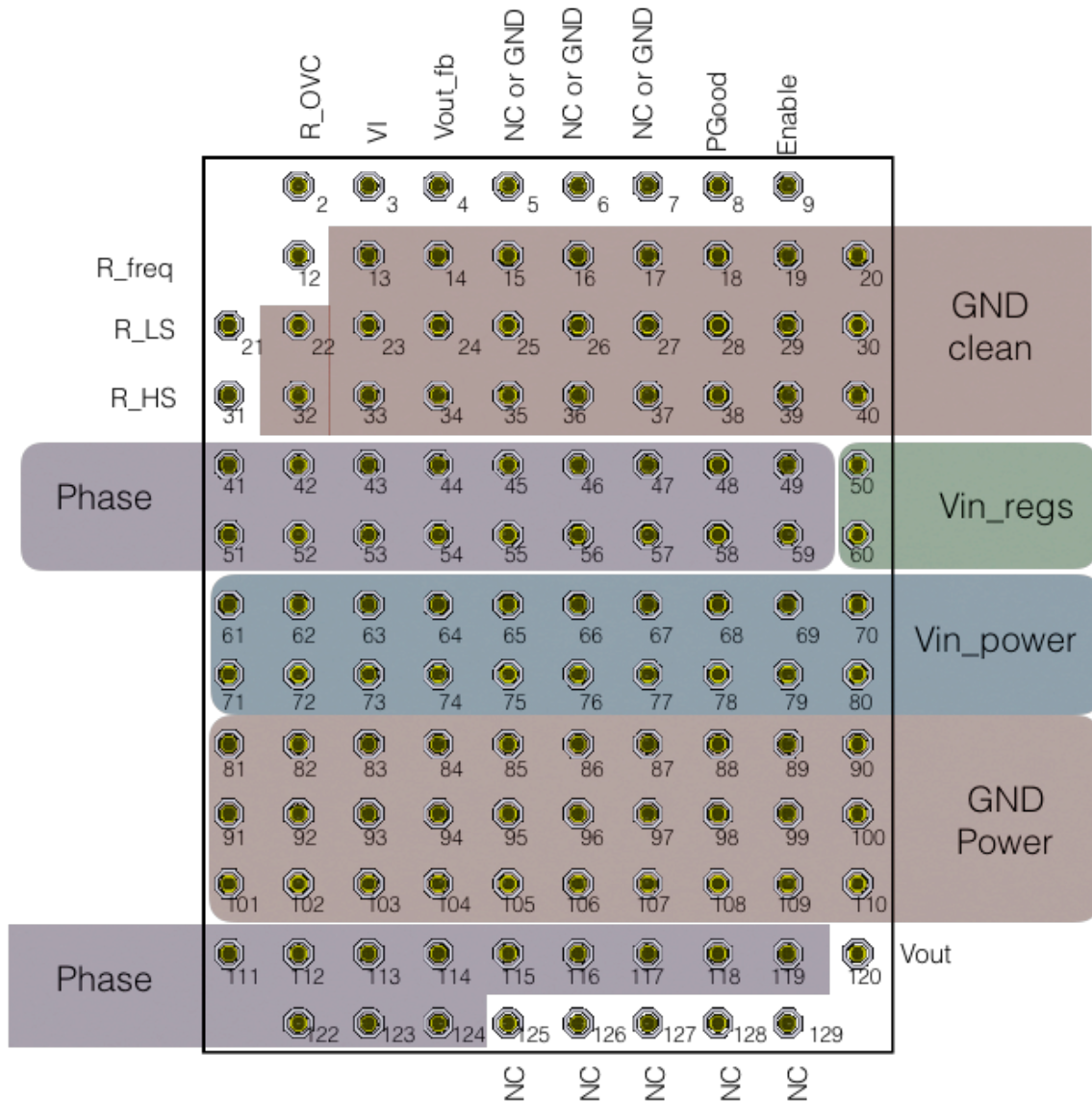


Figure 3: bPOL2V5\_V2.2 pin layout.

### Revision history

Revision	Date	Description
1.0	June 2016	First release of the document, pre-test
2.0	01/03/2018	Electrical and TID tests results added
3.0	16/04/2018	Pin numbering changed, as in G.Blanchot module
4.0	17/10/2018	Vin max increased to 1.5V