bPOL12V_V6

Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter

Features
- Input voltage range 5.5 to 12V
- Continuous 4A load capability
- Integrated Power N-channel MOSFETs
- Adjustable switching frequency 1-3MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Under-voltage lockout
- Over-Temperature protection
- Power Good output
- Enable Input
- Selectable Vout adjustment of +6.6%, -6.6% and -13.3%of the initial Vout value

Applications
Point Of Load in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

Description
bPOL12V_V6 is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment.
The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the converter capable of continuous operation up to HL-LHC outer tracker radiation limit (50Mrad and 1e15 n/cm^2). Maximum specifications with radiation are:

TID max	150Mrad	
SEE max	45 MeV/(mg/cm²)	
DD max	unbiased	7e15n/cm2 1.2e15p/cm2 (27MeV) 2.34e15p/cm2(230MeV) 4.71e15p/cm2(24GeV) 4e14p/cm2 (27MeV) + 6e14 n/cm2
	Biased	4.22e15 p/cm2 (24GeV) 0.6e15p/cm2 (27MeV)

bPOL12V_V6 has been designed for operation in a strong magnetic field in excess of 40,000 Gauss, and has been optimized for air-core inductors of 400-500nH: to be compatible with these small coil values, its switching operation is in the 1-3MHz range (1.3-2MHz for maximum efficiency).
The monolithic construction of bPOL12V_V6, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide POL regulation from a 5.5-12V supply rail. Its protection features include Over-Current, Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions. The chip temperature increase in the application can be monitored via a dedicated analog signal (PTAT).

Typical application L=460nH, fs=1.5MHz (used in ATLAS tracker applications)

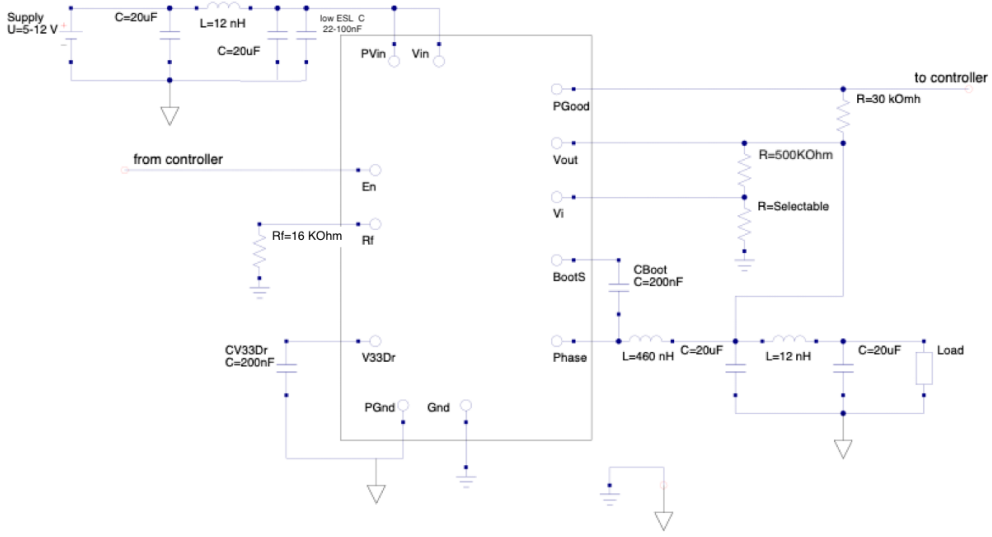


Figure 1a: typical application for fs=1.5MHz

Typical application L=220nH, fs=2.5MHz (used in CMS tracker applications)

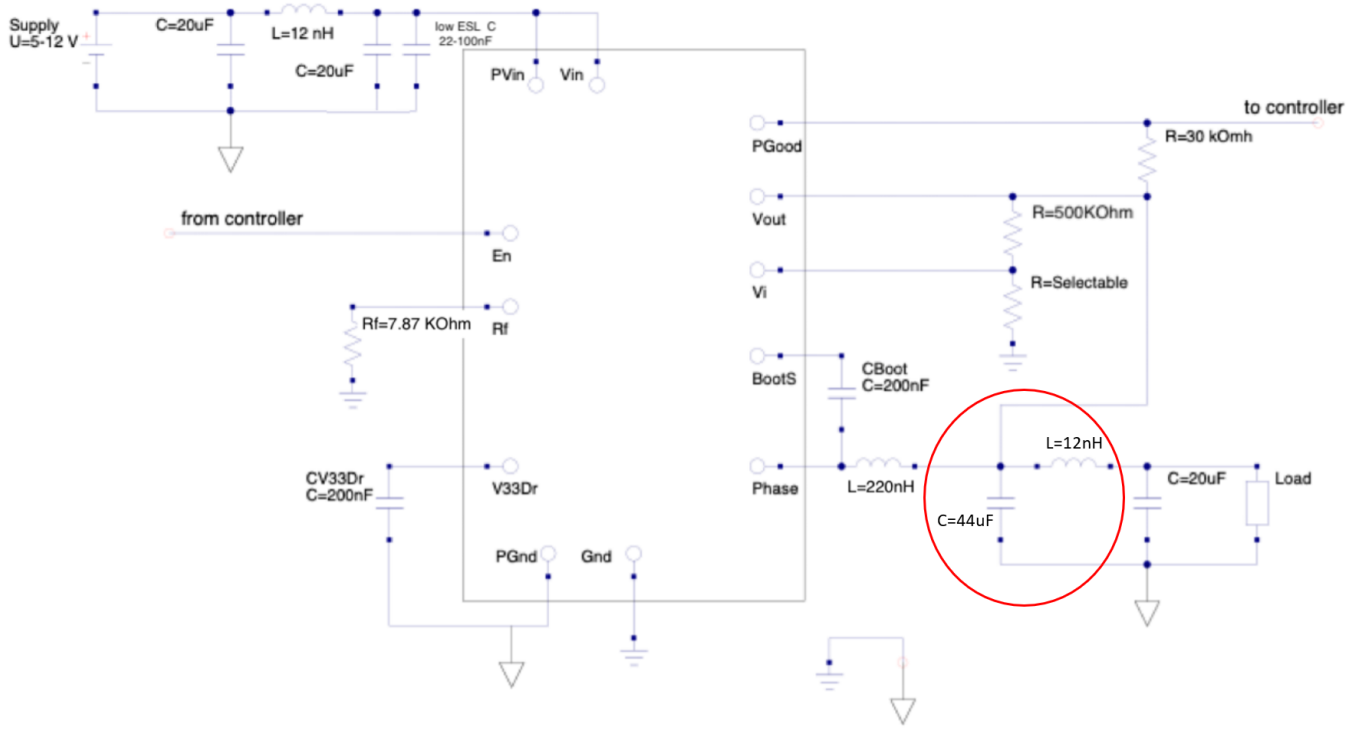
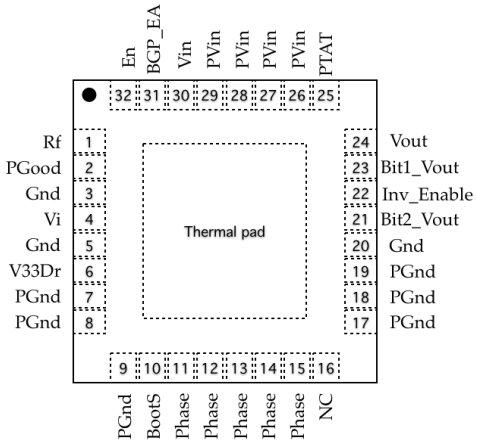


Figure 1b: typical application for fs=2.5MHz, please note that the output capacitor must be doubled for stability issue

Absolute Maximum Ratings

Power Input Voltage PVin……..….-0.3V to +12V
Control Input Voltage Vin……..……-0.3V to +12V
Bootstrap Voltage BootS……..…..-0.3 to PVin+3.6V
Phase Voltage…..….0.3 V to Vin (DC), -2 to 12 V (AC, 10ns)
Phase to BootS Voltage…….…..…-0.3V to +3.6V
Driver Voltage, V33Dr..……..……...-0.3V to +3.6V
Feedback input Voltage of the E/A Vi…….……-0.3V to +3.6V
Frequency selector Rf……..….-0.3V to +3.6V
Vout changer Bit1_vout and Bit2_Vout ……..….-0.3V to +3.6V
Reference voltage toggle Ref1V2……..…….-0.3V to +3.6V
Converter Enable En ……..……..……..-0.3V to +3.6V
Power good PGood……..……..……-0.3V to +6.0V
Output Voltage Vout……..……..……-0.3V to +6.0V
Current in PGood pin (when PGood is negated)…..…….50uA

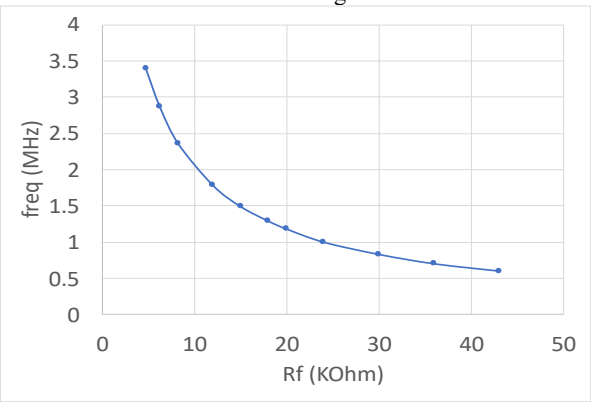
Pin Configuration



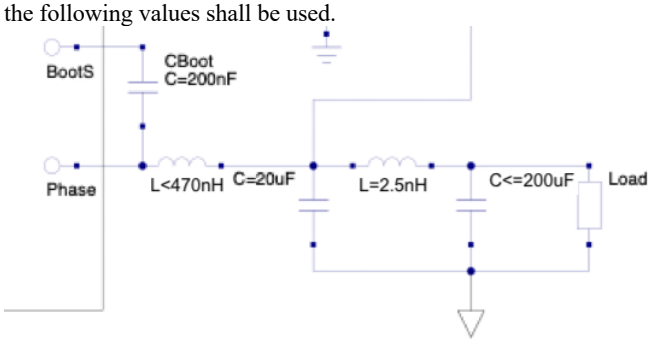
Top view - 32-lead plastic QFN (5x5 mm)
Thermal pad must be soldered to PCB PGnd

Pin Function

Rf (Pin 1): Frequency Selector. A resistor placed between this Pin and the board GND determines the switching frequency of the converter as illustrated in the following table.



The recommended range for best performance is 1.5-2 MHz. However, the switching frequency has to be adjusted, as a function of the selected inductor, to limit excessive peak-peak currents at every switching cycle that could affect long-term reliability. For 460nH inductor the suggested switching frequency is 1.8Mhz and for 220nH it is mandatory to have a switching frequency of at least 2.5Mhz. In other terms the product L*fs>550 MHz*nH. Maximum tested switching frequency is 3MHz.
The inductor however must be selected in the range 220nH -> 460nH. Higher values of inductors strongly affects the stability of the regulation loop. Please contact dcdc.asic.support@cern.ch for more info. Same issue for stability is present if the total output capacitance (including the one after the main undoctor, the capacitor after the PI filter and all the capacitors connected to the load) is exceeding 40uF. In this case the pi filter must be modified to ensure the stability (namely lowering the inductor from 12.5nH to 2.5nH).
For high value of capacitance attached to the Vout node (max 200uF) the following values shall be used.



For more informations please contact dcdc.asic.support@cern.ch. A model in Simplis can be provided to optimize the AC behaviour.

PGood (Pin2): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 500uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout.

Gnd (Pin3, 5, 20): Ground of the control electronics of the converter. It must be connected to the PCB ground plane possibly in a location remote to the power current loop in the same plane.

Vi (Pin 4): Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 150kHz, but the DC regulation voltage Vout is selected by the addition of 2 resistors building a voltage divider between Vout and gnd. Vi is connected between the 2 resistors and the resulting voltage is compared to the internal reference voltage. During the production lot Vref has been tested and the average value is 629mV with st. dev. of 8mV (calculated over 140k samples in August 2023, on the last production batch) therefore around 1.27% of its value. The Vout sigma is also 1.27%. The resistor between Vout and Vi must have a value of 500KΩ, while the one between Vi and gnd is selectable (no resistor makes Vout = Vref).
For the following Vout the suggested R2 (from Vi to GND) is:
Vout=3.3V, R2= 118KOhm, Vout=2.5V, R2= 169KOhm,
Vout=1.5V, R2=362KOhm, Vout=1.2V, R2= 552KOhm

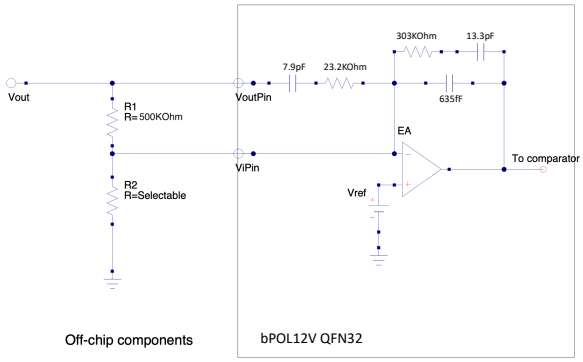


Figure 2: Configuring the output voltage.

V33Dr (Pin6): Voltage supply for the drivers of the power transistors. Although the regulator providing the 3.3V to the drivers is integrated, the large gate capacitance of the power switches requires a hefty charge storage element capable of providing quickly all the required transient current. This can not be achieved by on-chip capacitor, and an external capacitor of 220nF, positioned as close to the V33Dr pin as possible and directly connected to the PGnd (on the top PCB layer), is required.

PGnd (Pin 7, 8, 9, 17, 18, 19): Power Ground. This is the gnd of the power train and drivers, where large current transients are flowing. All PGnd pins must be connected to a large power plane under the qfn32, itself soldered to the Thermal Pad of the package, and connected to the PCB gnd plane by a large number of vias.

BootS (Pin 10): BootStrap capacitor voltage. bPOL12V_V6 uses 2 NMOS transistors in the power train, and the High Side (HS) switch requires a BootStrap circuit, which is embedded, for correct gate driving (the gate has to be connected to Phase for turn-off and to Phase+3.3V for turn-on). Given the large size of the HS power switch, an off-chip capacitor is required to provide the transient current to the HS drivers during switching. This capacitor, of 220nF, must be positioned between Phase and BootS pins, as close as possible to the qfn32 package.

Bit2_Vout (Pin 21): Pin to change the Value of Vout along with Pin23. If left floating the Vout is only determined by the voltage divider between Vout,Vi and GND.

Inv_Enable (Pin 22): Toggle of the polarity of the Enable pin. If this pin is connected to gnd, the polarity of the Enable pin is switched. It is recommended to leave this pin floating.

Bit2_Vout (Pin 23): Pin to change the Value of Vout along with Pin21. If left floating the Vout is only determined by the voltage divider between Vout,Vi and GND.

Vout (Pin 24): Regulated output voltage. This is an input pin bringing the Vout back to the converter's feedback circuit. It must be connected as specified in the description of Pin 4 (Vi).

PTAT (Pin 25): Proportional To Absolute Temperature provides and analog voltage whose variation with the chip junction T is linear with a slope of about 4.85mV/ºC. Maximum output current 15uA.

PVin (Pin 26, 27, 28, 29): Power Input Voltage. Input voltage of the power switches and drivers, where large current transients are flowing. Large input capacitances must be connected between this pin and PGnd as close to the package as possible and low-ESL capacitor has also to be putted (see board design recommendations later on).

Bgp_EA (Pin 31): The reference voltage to the Error Amplifier is buffered and made observable at this pin exclusively for test purposes. It is recommended to leave this pin floating.

Vin (Pin 30): Input Voltage for the control electronics of the converter. It is recommended to connect it to Pvin close to the chip.

En (Pin 32): Enable input. bPOL12V_V6 is normally disabled and requires a voltage above 800mV applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V. There is an hysteresis, to switch off bPOL12V_V6 the Enable pin must be lower than 500mV. The polarity of the pin can be inverted by connecting Inv_Enable (Pin22) to gnd, in which case bPOL12V_V6 is enabled for applied voltages below 800mV. Note that an embedded 15 kΩ resistor pulls the voltage of the En pin to gnd.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage – Pvin, Vin	5.5	11	V
Output voltage – Vout	0.63	5	V
Conversion ratio – Vout/Vin	2	10	
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	4	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	10	W
Switching frequency	1.5	2.5	MHz
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	ºC
Inductor value	220 at fs=2.5MHz	460 at fs=1.5MHz	nH
Inductor* switching frequency (L*fs)	550		MHz*nH
Enable voltage		3.3	V
Power Good voltage		3.3	V

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
Pvin, Vin	Input voltage supply range	Converter operational	5.5	6-11	12	V
Iin	Input current for control electronics (via Vin pin)	En pin low, converter disabled	-	8	-	mA
Iout *(note1)*	Output current	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	1	A
		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18ºC	-	-	4	A
Pout *(note1)*	Output power	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	2	W

		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18ºC	-	-	10	W
PWM						
Dmax	Maximum Duty Cycle		-	97	-	%
Dmin	Minimum Duty Cycle		-	0	-	%
Error Amplifier						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	20	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	10	-	V/µs
Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note2)*	-	5.5	-	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note2)*	-	5	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note2)*	-	800	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note2)*	-	500	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when bPOL12V_V6 is not powered)		-	0.1	-	kΩ
EnPullDownRes	Embedded Enable resistor to GND		-	15	-	kΩ
Protections						
OCPpk	Over Current Protection peak level	Vin=10V, Vout=1.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18ºC, *(note3)*	-	8.1	-	A
OCPavg	Over Current Protection average output current level	Vin=10V, Vout=1.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18ºC, *(note2, note4)* Vin=10V, Vout=1.5V, f=1.5MHz, L=460nH, Tcoolingpad≈18ºC, *(note2, note4)* Vin=10V, Vout=2.5V, f=2.5MHz, L=220nH, Tcoolingpad≈18ºC, *(note2, note4)*	-	6.45 6.15 5.5		A
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level	-	150	-	ºC
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level	-	120	-	ºC
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=10V, Vout=2.5V, f=1.8MHz, L=410nH, Tcoolingpad≈18ºC, *(note2, note5)*		520		us
Power Good						
OV	Output Over Voltage Pgood upper threshold			+6.5		%
UV	Output Under Voltage Pgood lower threshold			-6.5		%
Proportional To Absolute Temperature signal						
PTAT	Analog output voltage	Converter disabled, environmental T sweep		4.85		mV/ºC
PTAT Iout	output current from PTAT				15	uA

Notes

Note 1: Max rated output current only allowed if max output power is not exceeded.
Note 2: Average value taken from measurements on 10 samples from the production run.
Note 3: This value has not been measured precisely and is reported as approximate indication of the peak current detection for OCP. The peak value does not have relevant dependence on Vin and Vout.
Note 4: The OCP uses a peak detector, hence the average output current for OCP detection depends on the input and output voltages. In particular, the OCP detection current for Vin=10V is not significantly different for Vout of 2.5 to 5V, whilst it increases by about 10% at 1.8V and even further at smaller output voltages.
Note 5: The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

Block Diagram

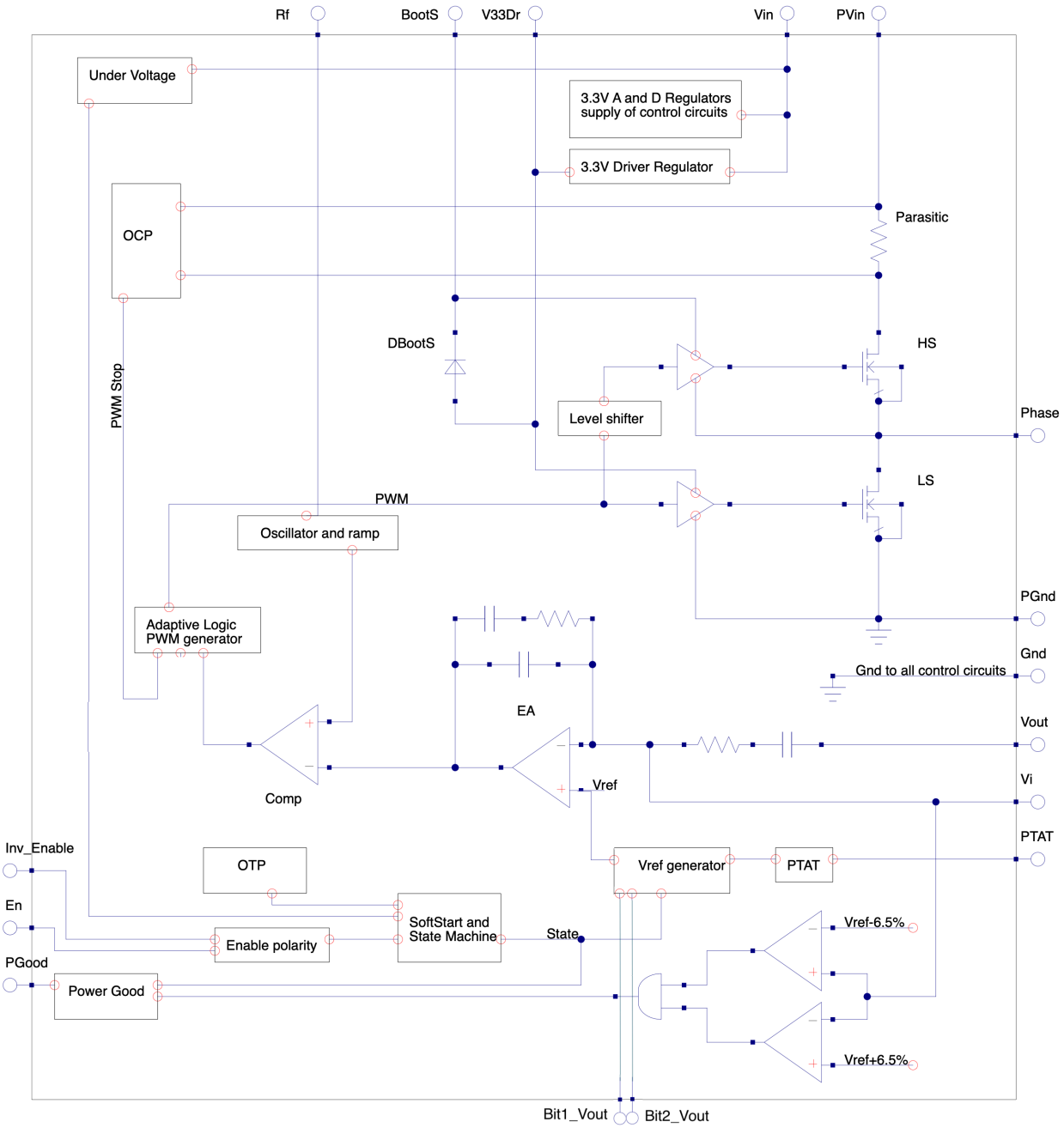


Figure 3: Block diagram of the bPOL12V_V6 ASIC.

Operation

bPOL12V_V6 is a DCDC converter designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace. The typical application at steady large load current with power provided from a remote supply (not from a battery) implies very relaxed requirements on quiescent current, while a fast feedback loop is at premium for some detectors where current consumption might have an instantaneous threefold increase.

bPOL12V_V6 has not been designed and tested for allowing large freedom in the choice of the external components (capacitors, inductors and resistors). Reliability for working at 11-12V is difficult to achieve and a long study in reducing the parasitic inductance between Vin and GND has been carried out. Extra low ESL capacitor (like the one in Figure 1 and 2 should be added in the PVin node. A module has been designed and files are available on EDMS at this address (https://edms.cern.ch/project/EDA-04466 for FEAST_MP like design and https://edms.cern.ch/project/EDA-04584 for FEAST_MP_CLP like design). A guide for the design of the module with explanation of the parasitic input current path is available here, as well as in the DCDC converter website, section modules.

Therefore it is strongly suggested that the design of the board must follow the design of this module. Please contact dcdc.asic.support@cern.ch for having more information on this module and design files.

Input voltage selection

Reliability of the bPOL12V family is a major concern for operation in the HL-LHC experiments. In particular the choice of the input voltage has a fundamental impact in the bPOL12V reliability.

Usually industry have a de-rating factor of 50%, meaning that if they have a high voltage (HV) devices that are rated 24V, the final product is rated only 12V. Usually the reliability tests are done on lots of around 100 samples for around 1000h at the defined voltage rating.

During the development of bPOL12V, it appeared that the only technology that can stand the level of displacement damage required by the experiment (1e15n/cm2) provides HV devices that can stand only 12V. Therefore a **disabled** (therefore without switching) bPOL12V can stand 12V as maximum input voltage. When bPOL12V is enabled, huge currents are switched in the power HV transistors, which are connected to the board through bond wires. Their intrinsic inductance, plus the parasitic inductance of the board and of the input capacitor, coupled with the fast-current transient results in voltage spikes, at each cycle, in the HV transistors.

In bPOL12V_V6 (with respect to previous prototypes), it has been decided to reduce the speed of the power transistor drivers in order to have softer commutation and less ringing in the Phase node, as shown in Figure 4. It is appreciable the reduction of the ringing, in particular in the rising edge: the Phase voltage never exceeds the input voltage.

Obviously, the price to pay is efficiency, since during commutation there is an increase of the conduction losses (higher resistance of the switches) and of the switching losses (longer simultaneous presence of current and voltage across the power transistors). It is therefore present a 1-3% loss of efficiency (depending on Vin and Iout conditions) with respect to bPOL12V_V4 and bPOL12V_V5 (as shown in Figure 5 and 6).

However, even if the Phase voltage is much smoother without overshoot, it is impossible to know exactly the amount of the internal voltage overshoot and its duration and even it would be possible, it is complicated to estimate the reliability, since in the technology manual reports only DC measures.

In this context we decided to run our proper reliability tests, with a rack that keep several enabled converters at a selectable input voltage, with different inductances and switching frequency (220nH and 460nH for 1.5MHz and 2.5MHz respectively) and different load (0A and 3.75A).

We tested two types of boards: one optimised by Pablo (optimisation present in the EDA-04466 and EDA-04584) with input parasitic inductance of 0.7nH and one as from previous developed FEASTMP board, with input parasitic inductance of 1.2nH.

The results are summarised in the following table

bPOL12V version	# devices	Vin (V)	Lpar board (nH)	Test days	Number of failed devices	Number of damaged devices (still running)
V3	70	12-13	1.22	250	16	0
V4	140	12	1.22	370	2	0
V5	150	11-12	1.22	400	70	0
V6	32 (0A) 31 (4A)	12	1.22	1073 (on going)	0	0
	16 (0A) 16 (4A)	12	0.7	880 (on going)	0	0
	16 (0A) 15 (4A)	13	1.22	187 STOPPED	0	11 soft (only 4A, first after 37 days)
	30 (0A) 28 (4A)	13	0.7	880 (on going)	0	0

From the table it is evident that at 12V there is no single failure for almost 2 years, independent on the type of PCB used (lower or higher inductance). At 13V we never had failure with the optimised board (0.7nH) but we saw rapidly damage (only 37 days) with the non-optimised board (1.2nH). This is clearly the sign that at 13V we are really close to the reliability limit, and the accurate design of the PCB matters a lot.

Summarising the bPOL12V can be run safely at 12V with optimised board. It can stand 13V during transient in the system with optimised board.

No more than 13V shall be applied, there is no data on that and there will not be.

In conclusions:

recommended voltage is 11V,
bPOL12V can work reliability at 12V,
bPOL12V can stand in transient voltages up to 13V

Reliability tests are still on-going and updates will follow regularly.

Additional reliability test carried out by users

Additionally a large reliability work has been carried out by Tomasz Gadek which kindly accepted to share his results. A big thank to him. A population sample of 96 DC-DC converters built with bPOL12v6 ASICs was used in a reliability demonstration test to qualify the ASIC and the converter's design for use in the CMS MTD-BTL project over a time span of 20 years. Parameters of the test a target reliability of 0.995 at 95% confidence level for a mission profile of 200 thermal (-30°C to 70°C) and 400 power cycles (0 to 12 V). The test was crafted according to the Design of Experiment principles

with a multifactorial approach to save testing time and provoke failure modes originating from the interplay of different stressors. The convoluted stresses from multiple sources: thermal, power and load cycles acted simultaneously with vibrations quantified on the specimen to be in the range of 0.07 to 0.12 g in all 3 axis, with occasional peaks, measured approximately once an hour, up to 0.25 g in Z-axis (along the Earth's gravitational force vector). The power and load cycles happened at the temperature extremes after 10 minutes of dwell time. Test time was calculated based on Weibull distribution approximation of a failure rate with a shape parameter β = 1.0, assuming a'priori no wear-out mechanism and the source of infant mortality in the cohort being only patent defects weeded out in the factory acceptance testing and not being present in the test sample population. At 0 observed failures the estimated test time was 1245 thermal and 2490 power cycles. The test was extended beyond that target lasting 1401 thermal and 2802 power cycles, pushing the reliable operating time span, under stated conditions, to 22.5 years.

# of bPOLs	Powering strategy	Regulated voltage	Load	Thermal cycles	Power cycles (0 – 12 V)	Observed failures
96	48: powered continuously during temperature ramps	8: 1.26 V	1: 3.0 A	1401	2802	0
			7: 0.0 A	1401	2802	0
		8: 2.57 V	1: 3.0 A	1401	2802	0
			7: 0.0 A	1401	2802	0
		32: 1.80 V	6: 4.0 A	1401	2802	0
			26: 0.0 A	1401	2802	0
	48: powered only at temperature extremes	8: 1.26 V	1: 3.0 A	1401	2802	0
			7: 0.0 A	1401	2802	0
		8: 2.57 V	1: 3.0 A	1401	2802	0
			7: 0.0 A	1401	2802	0
		32: 1.80 V	6: 4.0 A	1401	2802	0
			26: 0.0 A	1401	2802	0

Additionally, the over temperature protection circuitry was tested on the above population of converters in 20 thermal cycles from 50°C to 90°C ambient. The PCB temperature of loaded converters reached beyond 100°C at 90°C ambient and beyond 64°C at 50°C ambient. All loaded converters would enter the OTP mode beyond PCB temperature of 100°C and fully recover their operation at lower temperatures.

Data from reliability test is openly accessible here: https://eth.app.cern.ch/pcc_reliability_search.php

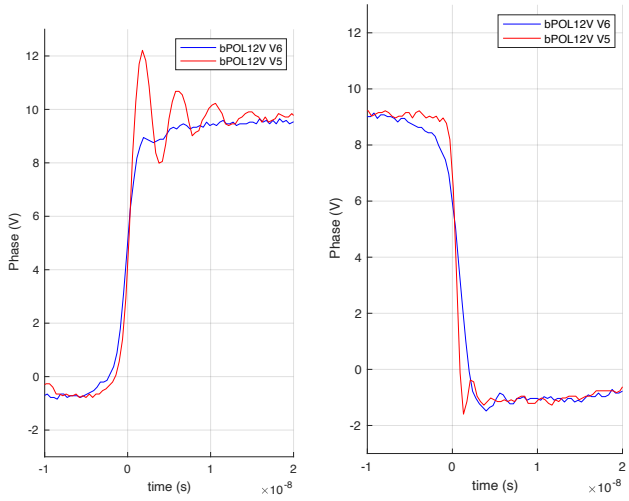


Figure 4: Phase node for bPOL12V V6 and V5, rising edge on left side and falling edge on right side, Vin=10V, Iout=4A and L=460nH.

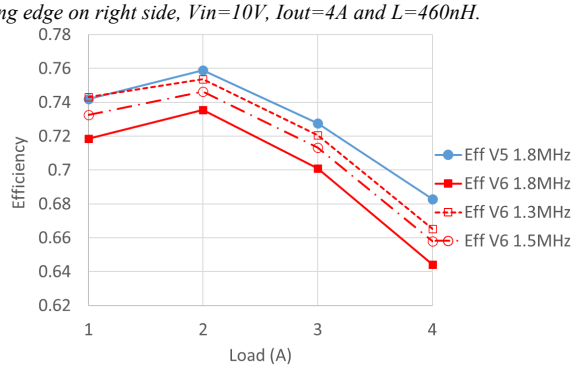


Figure 5: Efficiency difference between bPOL12V V6 and V5 Vin=10V, L=460nH, Vout=1.5V.

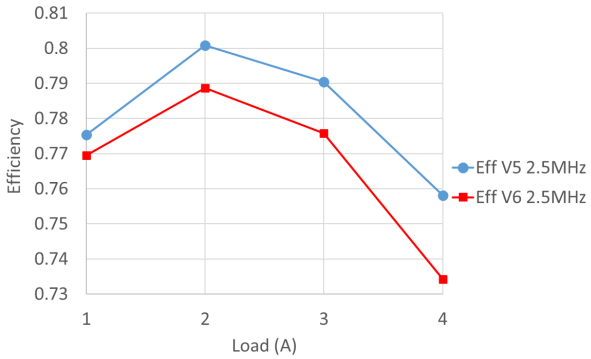


Figure 6: Efficiency difference between bPOL12V V6 and V5 Vin=10V, L=220nH, Vout=2.5V.

Output voltage selection

The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage (Vref) to the Error Amplifier. Different production lots have been tested and the average value of the Vref is 632mV with st dev of 7mV (calculated over production lots of 3k ASICs in January 2022, 22k ASICs February 2022 and 140k samples in August 2023)

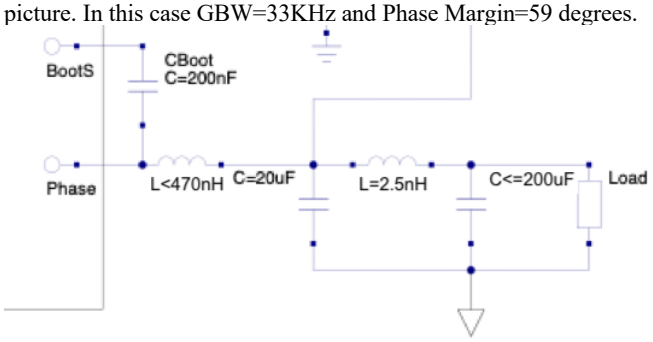
The formula to calculate the proper R selectable for a wanted Vout Vout and given the Vref as above is:
Rsel=500KOhm*Vref/(Vout-Vref)
With the two pins Bit1_Vout and Bit2_Vout is it possible to slightly change the value of the Vout as follows:

Bit1_Vout,Bit2_Vout	Vout
0,0	nominal
0,1	-13.3%
1,0	-6.67%
1,1	+6.67%

Where 1 is the high value of Bit*_Vout. The pin threshold is 0.7V.
If the two Bit*_Vout pins are left floating the Vout is simply generated with the voltage divider.

Switching frequency
The switching frequency of the converter can be adjusted with one external resistor, which provides the bias current to the embedded oscillator. Although bPOL12V_V6 has been tested as functional over a wide range of frequency (1 to 3.5MHz), best performance is achieved in the range of 1.5-2MHz. At lower frequency, the peak-to-peak current in the small air-core inductor increases excessively and determines useless losses and possibly an early onset of the OCP. At higher frequency, driving losses increases dramatically and make the efficiency drop very sensibly.
For a 460nH range inductor, the suggested switching frequency is 1.5MHz, where there is the best trade-off between reliability, efficiency and noise emission.
For some volume-limited application customers may use a 220nH inductor. It is anyway strongly suggested to use a higher value of inductance to decrease the peak-to-peak current that could affect long-term reliability. An inductance of 220nH requires a switching frequency of at least 2.5MHz. In other terms the product L*fs must be bigger than 550 MHz*nH.

Stability over frequency
The feedback loop of the bPOL12V has been optimized for the two configurations shown in Figure 1.a and Figure 1.b.
In this case the BGW is around 100KHz and the Phase margin around 70 degrees.
For any additional capacitance of the output node exceeding 40uF (therefore 20uF more than the depicted capacitance) or the use of higher value inductance must be carefully studied. As a guidance for a L<460nH and an output capacitance which is lower than 200uF, then the configuration that shall be used is depicted in the following picture. In this case GBW=33KHz and Phase Margin=59 degrees.



Embedded linear regulators
While it can operate from a supply voltage of up to 12V, the control electronics in bPOL12V_V6 requires powering at 3.3V. A number of linear regulators are embedded to provide appropriate voltage to the drivers of the power transistors, to the bandgap and reference current generator, to the analog and to the digital circuitry. With the exception of the voltage regulation for the power transistors' drivers, all storage capacitors required for the regulators are on-chip and have been sized to ensure steady voltage even during large current surges.

Under-Voltage lockout
The embedded linear regulators need a sufficient level of over-voltage to provide stable 3.3V voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above about 5.5V (on rising Vin). This comparator has a hysteresis and bPOL12V_V6 is disabled again when, for falling Vin, the input voltage drops below about 5V.

Enabling bPOL12V_V6
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has not been asserted by applying a voltage above about 800mV. On Enable pin there is an hysteresis of 300mV, therefore bPOL12V_V6 will turn off when Enable pin's voltage is under 500mV. bPOL12V_V6 can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each bPOL12V_V6 providing regulated power to a different load). bPOL12V_V6 is disabled by default if the En pin is floating – an internal pull-down resistor of 15 kΩ keeps the voltage of the pin to gnd.
The polarity of the enable signal can however be inverted by connecting the Inv_Enable pin to gnd. In this case, the circuit is disabled when a voltage above 800mV is applied to the enable (En) pin and vice versa the circuit is enabled when a voltage below 500mV is applied; it is hence enabled by default if the En pin is floating – an internal pull-down resistor of 15 kΩ keeps the voltage of the pin to gnd.

Soft Start procedure
When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the EA, the output voltage reaching the nominal value in about 520us in the nominal configuration using the 0.6V bandgap (at the switching frequency of 1.8MHz, this time varying inverse linearly with frequency). Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that bPOL12V_V6 is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 3.3V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, in reset and when the output

voltage is outside a ±6.5% window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 500uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PG pin is 3.6V.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip junction temperature and disables bPOL12V_V6 when it reaches about 120ºC. The OTP has a hysteresis of about 40ºC, hence the converter restarts (with SS) when the junction temperature decreases below 80ºC. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

Over-Current Protection (OCP)
OCP is integrated as a real peak detector on the current flowing during each cycle in the HS transistor. Current sensing takes place on the parasitic resistance of metal lines bringing the input current from the input pads to the HS transistor. When the instantaneous current exceeds about 8.1 A, the PWM is reset and forces the HS to turn off. If the excessive load current condition persists, the on-time of the HS is not determined anymore by the feedback loop (which would require longer on-times to provide more output power) but by the OCP, and as a consequence the output voltage drops. This condition might endure as a steady state, PG being pulled to gnd if the output voltage drop exceeds 6.5% of the nominal. The peak current of 8.1A translates in different average output current depending on the input and output voltage, frequency and inductor value.
For example, for a typical application Vin=10V, Vout=1.5V, fs=1.8Mhz. L=460nH the OCP average limited output current is around 6.45A. For Vin=10V, Vout=2.5V, fs=2.5Mhz. L=220nH the OCP average limited output current is around 5.5A.

Compensation network
The compensation network is fully integrated and determines a typical loop bandwidth of about 150kHz in the recommended operation environment (frequency, voltages, inductor, on-board passives). bPOL12V_V6 is hence capable of quickly adjusting the output voltage in case of output load transients.

Cooling
bPOL12V_V6 is specified for operation up to 10W output power. With an efficiency of 80% in case of large load current and not–cryogenic cooling, this translates in more than 2W lost in the converter (including the resistance of the inductor and of other passive components). Most of this power is burnt by bPOL12V_V6 itself and needs to be transferred to the cooling system efficiently. The chosen qfn32 package has an exposed cooling pad to which the IC is directly attached, and the pad must be soldered to the gnd plane of the PCB which itself must have a good thermal contact to the cooling system.

Proportional To Absolute Temperature (PTAT) voltage

The PTAT analog signal can be used to monitor the T increase of the bPOL12V_V6 ASIC during operation, in particular to verify that the cooling is appropriate. The absolute value of the PTAT voltage at a given T has a wide sample-to-sample variability. However, the PTAT increase with respect to T is very close to a straight line with slope 4.85 mV/ºC. This has been verified on 7 samples: although the PTAT value at the same T could vary by 200mV, all samples had a linear dependence between **Δ**PTAT and **Δ**T, with a very similar slope (averaging 4.85 mV/ºC). This linear relation is shown for one of the measured samples in the figure below.

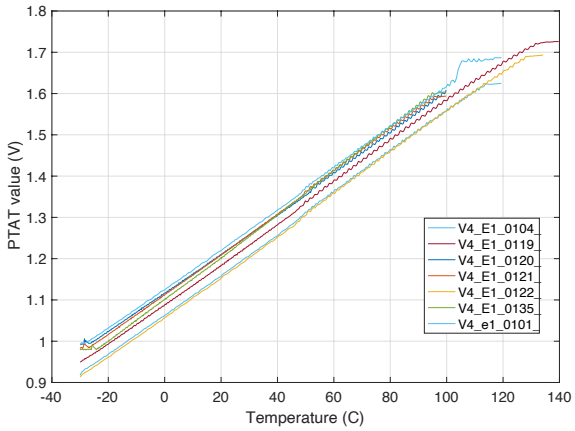


Figure 7: PTAT voltage.

Radiation tolerance

bPOL12V_V6 has been measured with different X-rays for TID effects and bPOL12V_V5 has been tested for displacement damage in reactor neutrons and 24GeV/c protons for displacement damage, Heavy Ions for SEEs. Other than directly on bPOL12V_V6, these tests have been done on several generations of prototypes of the converter ASIC, obtaining very comparable results for TID and displacement damage.

Total Ionizing Dose
Samples have been exposed under bias at 25ºC and -30ºC, while biased at 10V input voltage and providing 2A current to a load. The radiation source was the CERN X-ray irradiation system accelerating 40keV electrons on a Tungsten target. Different dose rates are used . An efficiency drop is the most evident effect, but it is limited to a 3-4% decrease in the worst case (without considering annealing, which improves the performance), mainly due to the leakage current appearing in the high voltage transistors that cannot be modified with enclosed layout geometry. The oscillations in the efficiency curves are due to annealing that occurs during the test of the UVLO (10 seconds). During this period of time the converter is disabled, annealing occurs and the leakage current reduces, improving the efficiency.
Regulation performance is only slightly affected above 100Mrad(SiO_2). Thresholds of the UVLO, OCP, OTP systems are affected as follow after Mrad(SiO_2):

- UVLO: negative shift of 100-200mV (shown in Fig 14-15)
- OCP: 0.1-0.3A
- OTP: OTPStartTh =90C and OTPStopTh=60C

PTAT suffers a more sever shift, around 300mV over 100Mrad as shown in Figure 13.
The enable thresholds have a shift depending on the dose rate and voltage on the Enable pin as shown in Figure 16.

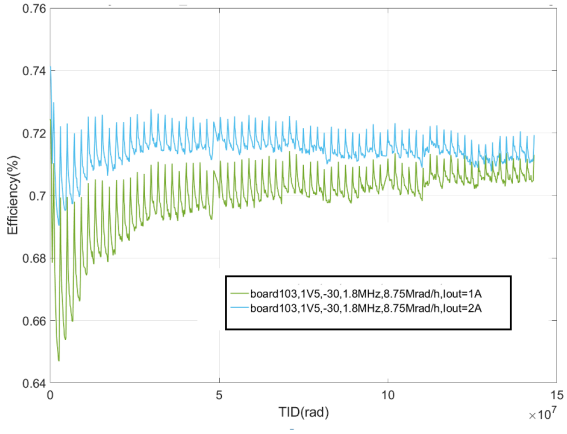


Figure 8: Efficiency variation with X-ray irradiation at the temperature of –30°C, for Vin=10V, Vout=1.5V, L=460nH, fs=1.8MHz.

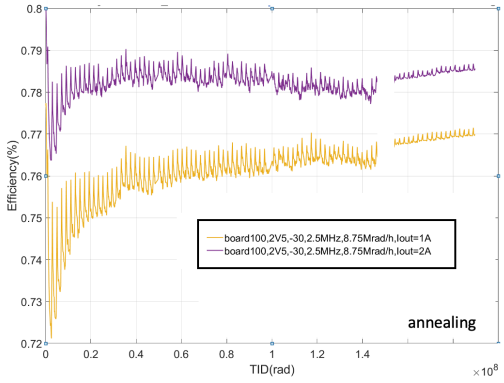


Figure 9: Efficiency variation with X-ray irradiation at the temperature of –30°C, for Vin=10V, Vout=2.5V, L=220nH, fs=2.5 MHz.

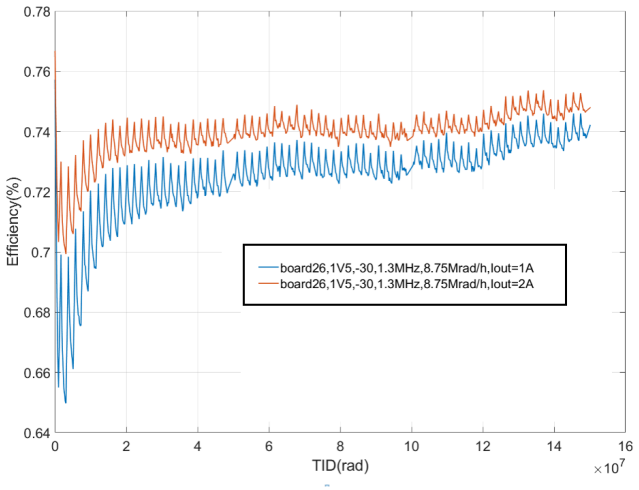


Figure 10: Efficiency variation with X-ray irradiation at the temperature of –30°C, for Vin=10V, Vout=1.5V, L=460nH, fs=1.3MHz.

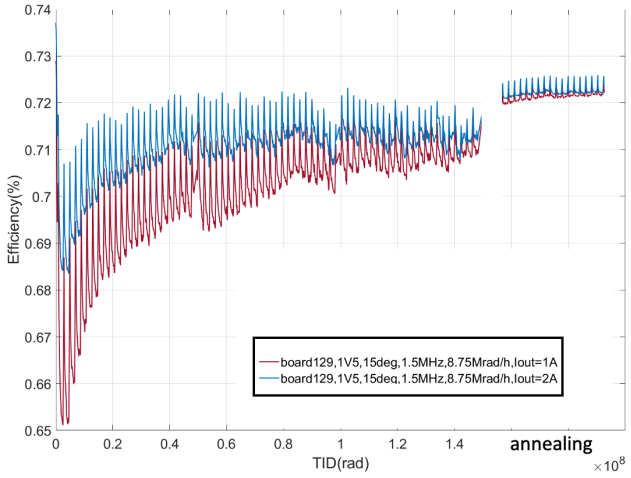


Figure 11: Efficiency variation with X-ray irradiation at the temperature of 15°C, for Vin=10V, Vout=1.5V, L=460nH, fs=1.5MHz.

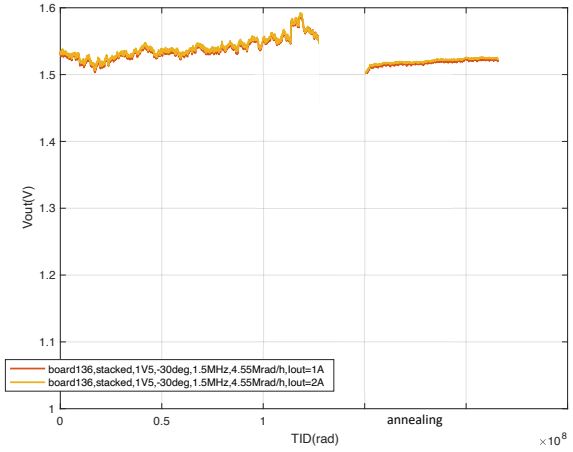


Figure 12: Vout variation with X-ray irradiation at the temperature of -30 °C, for Vin=10V.

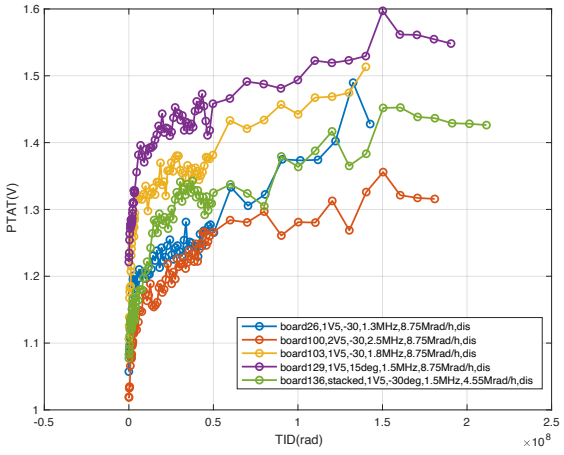


Figure 13: Ptat variation with X-ray irradiation at different temperatures for Vin=10V.

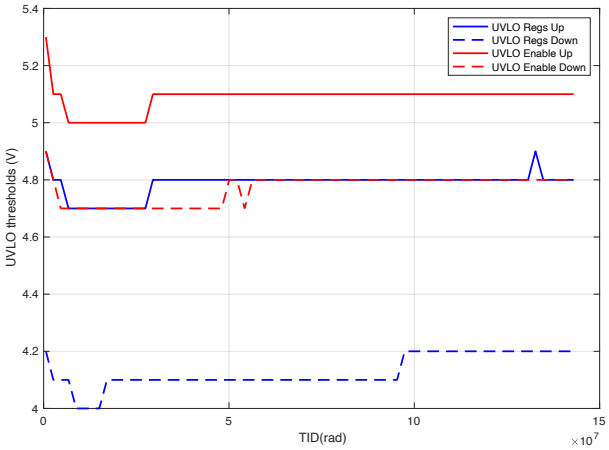


Figure 14: UVLOs variation with X-ray irradiation at the temperature of -30°C

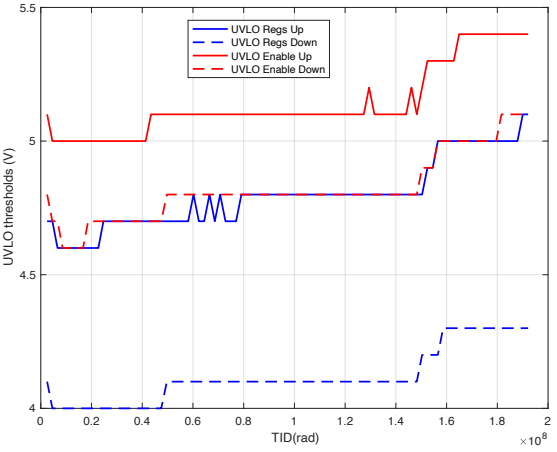


Figure 15: UVLOs variation with X-ray irradiation at the temperature of 15°C

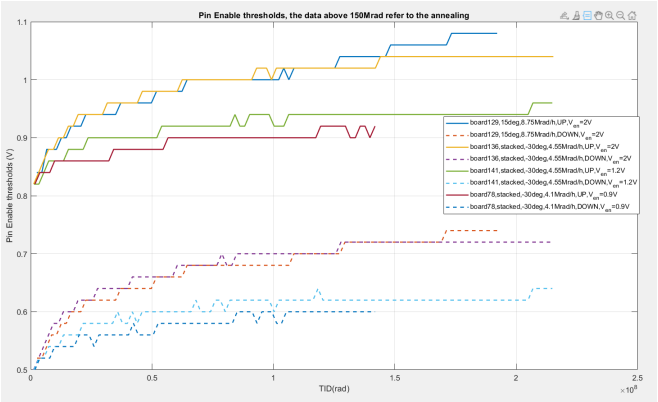


Figure 16: Enable threshold variation with different X-ray irradiation. The shift of the Enable threshold is strongly dependent on the voltage on the Enable pin. At 50Mrad and with Enable=0.9V the shift is limited to 50mV.

Displacement Damage

Displacement damage (DD) effects have been measured on bPOl12V_V6 and on previous prototypes during the development of the ASIC (bPOL12V_V5).

The limit flux for failure is not known precisely. In tests at a nuclear reactor (Triga at JSI in Ljubljana) samples were working at 7e15 n/cm^2. In tests at the 25-27MeV proton beam at Birmingham MC40 cyclotron samples were working at a fluence of 1.2e15p/cm2. In tests at the 230MeV proton beam at the Boston general hospital were working at a fluence of 2.34e15p/cm2. A double irradiation (protons + neutrons) has been also made on samples using the 27MeV MC40 proton beam + Triga neutron reactor beam for a fluence of 4e14p/cm2 + 6e14n/cm2. Also these samples were working. In the CERN IRRAD facility, with the proton beam at 24GeV unbiased devices have been tested. Biased device have been irradiated, but the results are difficult to interpret due to the high flux of particle (~7e12 p/(s cm2), around 5-6 order of magnitude higher than the flux in tracker and forward calorimeters of LHC experiments). Multiple Events have been seen and not representative for the final application. Under bias bPOL12V_V6 was operative up to 4.22e15 p/cm2. The V33driver output of the linear regulator went down to 200mV. It has been kept under irradiation and under bias up to 7e15 p/cm2 (V33driver=0V). After annealing at 100C for 1 week the bPOL12V_V6 was back operative.

A test under bias has been also carried out by RWTH Aachen in Cyrce proton beam 27MeV up to 0.6e15p/cm2 without any sensible issue.

The following Table provides more detailed information of the dosimetry of the above-mentioned irradiations. All samples are operatives.

particle	source	Energy	fluence (particle 1e15/cm2)	1MeV equivalent e15	TID (Mrad)	number of samples	bias?	version tested	notes
neutrons	Triga	<10 MeV	2.00	2.00	2	2	unbiased	V5	
			5.00	5.00	5	2	unbiased		
			6.00	6.00	6	2	unbiased		
			7.00	7.00	7	2	unbiased		
neutrons	ouvain la Neuve		0.28	0.28		1	biased Vin=10V, enabled	V5	
otons+neutro	MC40+Triga		0.4p+0.6n	1.48	54	4	unbiased	V5	
protons	MC40	27 MeV	0.41	0.91	108	6	unbiased	V5	
			0.53	1.16	137	6	unbiased		
			0.65	1.43	169	6	unbiased		
			0.90	1.98	234	5	unbiased		
			1.20	2.64	312	5	unbiased		
protons	Boston GH	230MeV	1.43	0.95		2	unbiased	V5	
			1.82	1.21		2	unbiased		
			2.34	1.55		2	unbiased		
protons	IRRAD	24GeV	0.90	0.50	24	4	unbiased	V6	
			1.91	1.06	52	4	unbiased		
			2.41	1.34	66	4	unbiased		
			2.86	1.59	78	2	unbiased		
			3.07	1.71	84	2	unbiased		
			4.71	2.62	128	2	unbiased		
			4.58	2.54	125	1	biased =0, turned on every 5 min	V6	V33driver drops, irradiaeted up to 7e15p/cm2, 1 week of annealing 100C, back operative
			4.22	2.34	115	1	ased Vin=10V, enable	V6	
protons	Cyrce	27 MeV	0.53	1.166	150	1	Biased Vin=9V	V6	still operative , thanks to RWTH Aachen
			0.6	1.32	171.4	1			

The most appreciable shift of the converter parameter is the Over Temperature protection threshold (OTP). For applications hitting the 9e14p/cm2 fluence, the shift to be expected is important, decreasing to 70C (measured after annealing at room temperature for months).

The shift in efficiency is in ±1% range, which is in the ASIC-ASIC efficiency variation. Therefore, we can assume that there is not a sensible degradation of the efficiency due to displacement damage.

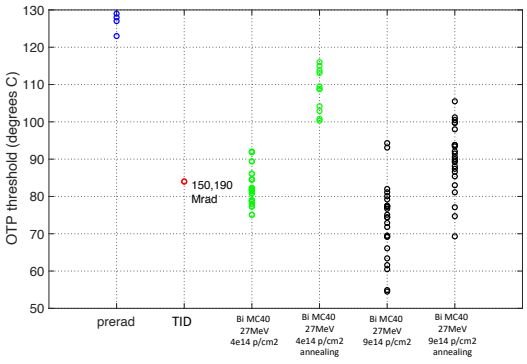


Figure 17a: OTP threshold variation with different source (TID and 27MeV proton beam on MC40, Birmingham).

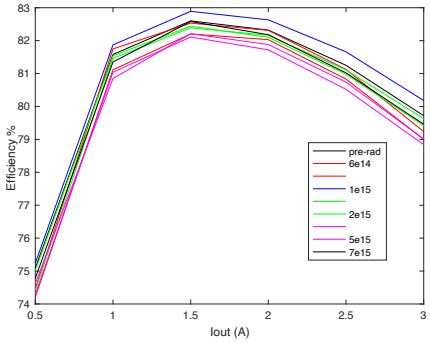


Figure 17b: Efficiency vs Iout at different fluence (n/cm2) for neutron irradiation in Triga reactor. Vin=10V, Vout=2.6V, f=1.8Mhz, L=460nH. Vin and Vout are taken at mother-board level due to setup restrictions with irradiated board. Pre-rad board is a board not irradiated working in the same conditions and in the same setup for comparison.

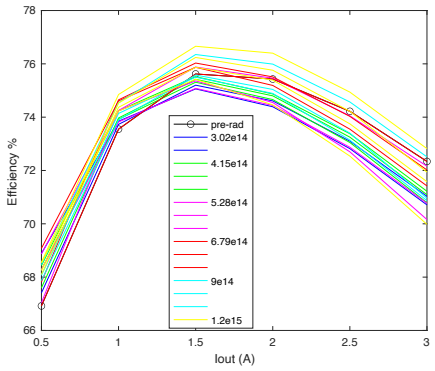


Figure 17b: Efficiency vs Iout at different fluence (p/cm2) for 27MeV proton irradiation (27MeV proton beam on MC40, Birmingham). Vin=10V, Vout=1.5V, f=1.8Mhz, L=460nH.

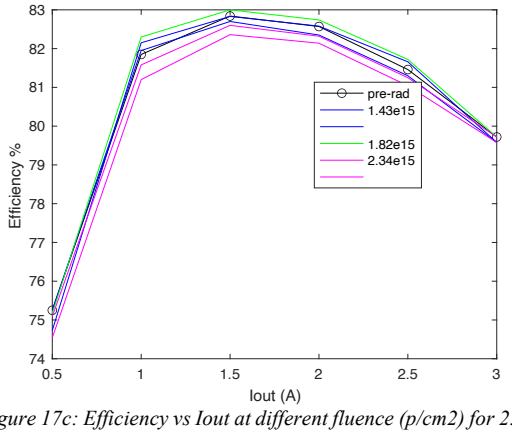


Figure 17c: Efficiency vs Iout at different fluence (p/cm2) for 230MeV proton irradiation (230MeV proton beam at the Boston general hospital). Vin=10V, Vout=2.6V, f=1.8Mhz, L=460nH. Vin and Vout are taken at mother-board level due to setup restrictions with irradiated board. Pre-rad board is a board not irradiated working in the same conditions and in the same setup for comparison.

Single Event Effects

SEEs have been measured on previous prototypes during the development of the ASIC, but the result summarized hereafter are representative since the circuits affected have not been modified in bPOL12V_V6. SEE have been measured with a Heavy Ion beam at CRC, Louvain-la-Neuve on different samples also with pre-irradiated TID (100Mrad for bPOL12V_V5, 200Mrad,250Mrad and 300Mrad for bPOL12V_V3) and pre-irradiated with displacement damage (2e15 and 5e15 n/cm2 on bPOL12V_V3).

Details on the irradiated samples, operating voltages, ions used and tilt, are reported in following Table.

	source	version tested	b name	Vin	Vout	eq LET	Milion ions	Ion	tilt
200Mrad	Xray CERN	V3	36	10	2.5	16	10	Cr	
						32	3.6	Kr	
250Mrad	Xray CERN	V3	25	10	2.5	16	4.4	Cr	
300Mrad -30C	Xray CERN	V3	SA3	10	2.5	16	9.2	Cr	
						23	4.6	Cr	45
						32	1.45	Cr	60
						32	2	Kr	
2e15n/cm2	N Triga	V3	N2	10	2.5	16	12	Cr	
						32	3.8	Cr	60
						32	5	Kr	
5e15n/cm2	N Triga	V3	N5	10	2.5	16	5	Cr	
150Mrad -30C	Xray CERN	V6 stacked	141	12	1.5	16	5	Cr	
						46	5	Rh	
150Mrad 15C	Xray CERN	V6	129	12	1.5	16	5	Cr	
150Mrad -30C	Xray CERN	V6	100	12	2.5	46	5	Rh	
not irradiated		V6 stacked	98	12	2.5	16	5	Cr	
						46	2	Rh	
		V6 stacked	95	12	2.5	4.67	5	Ne	45
						5.7	10	Al	
						8	5	Al	45
						11.4	5	Al	60
						16	5	Cr	
						23	5	Cr	45
						32.4	2.5	Kr	
						46	5	Rh	
		V6	134	12	2.5	16	5	Cr	
		V6 stacked	126	12	1.5	3.3	7.5	Ne	
						4.67	5	Ne	45
						5.7	10	Al	
						8	5	Al	45
						9.47	5	Al	53
						16	5	Cr	
						23	5	Cr	45
						32.4	3	Kr	
						37.4	5	Kr	30
						46	5	Rh	

There is no remarkable difference in the SEE susceptibility between the different samples. The highest LET was from the krypton ion, with 32 $MeVcm^2mg^{-1}$ at normal incidence and with 37.5 $MeVcm^2mg^{-1}$ at 30 degree incidence. No destructive event has been recorded when exposing the sample to 5e6 krypton ions/cm^2 . Short transients where the Vout changed by about 200-300mV for less than 3us were observed at the output, that was regulating 2.5V with 1A load with an inductance of 460nH and switching frequency of 1.8MHz.

With an inductance of 220nH, 2.5Mhz and Vout=2.5V, Iout=1A the short transient are in the range of 500-600mV.

These events, with a cross-section of 6.8e-6 cm^2, are negligible for practical applications. No functional interrupts (SEFIs) were also observed .

Details of the waveforms are reported in the following pictures. There are two type of transients: short (1-2us) and long (~20us) but with reduced amplitude.

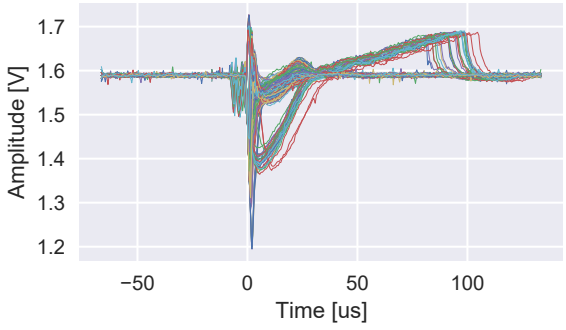


Figure 18: Typical waveforms for Vout=1.5V and LET=16 $MeVcm^2mg^{-1}$

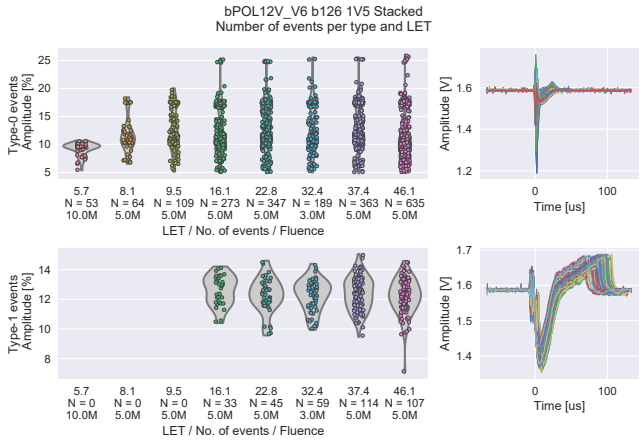


Figure 19: Typical waveforms for Vout=1.5V configuration. Upper part is related to the "fast" transients, 1-2us, lower part is "long" transient. On the right side there are examples of the waveforms superposed, while on the left there is the maximum amplitude in % of the Vout per LET of the detected transient.

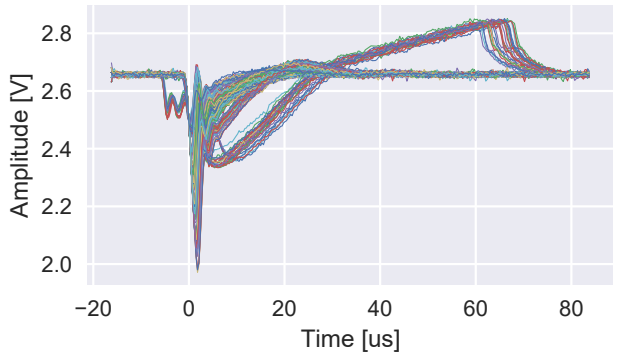


Figure 20: Typical waveforms for Vout=2.5V and LET=16 MeVcm^{2}mg^{-1}

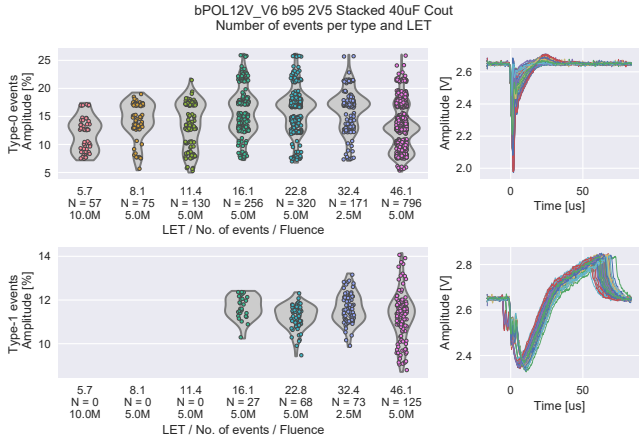


Figure 21: Typical waveforms for Vout=2.5V configuration. Upper part is related to the "fast" transients, 1-2us, lower part is "long" transient. On the right side there are examples of the waveforms superposed, while on the left there is the maximum amplitude in % of the Vout per LET of the detected transient.

Typical operation waveforms

The figures in this section have been taken on a single module from a pre-production run using the bPOL12V_V6 ASIC using the board described in page 7. The results are mainly reported for the 2.5V (CMS tracker and ATLAS EOS application) and 1.5V version (Atlas ITK applications).
The 2.5V version has a switching frequency of 2.5MHz and 220nH main inductor (coilcraft 132-12L).
The 1.5V version has a switching frequency of 1.5MHz and 460nH main inductor (coilcraft 132-17L).
The inductors are solenoid for these tests for simplicity and availability of the samples. It is strongly suggested to use toroidal inductor in CERN experiment application with on top a 100um Al shield, to limit the radiated noise.
The main electrical parameters of these inductors are reported in the below table

Part number	Inductance (nH) ±5%	Q min	DCR max (mΩ)
132-13L	246	70 @ 25 MHz	20.3
132-17L	460	66 @ 25 MHz	22.5

The presence of the input and output π filter inductors (both 12nH in Figure 1.a) plays a role in the efficiency and load regulation due to their intrinsic series resistance.
Therefore, in the followings, plots of the ASIC performance without the input+outout filters will be presented along with the plots with the input+outout π filters which will provide a more precise idea of the performances of the full PCB module.
The presented results are typical of a fresh (not irradiated) sample: for radiation-induced degradation please refer to the previous section (Radiation tolerance).

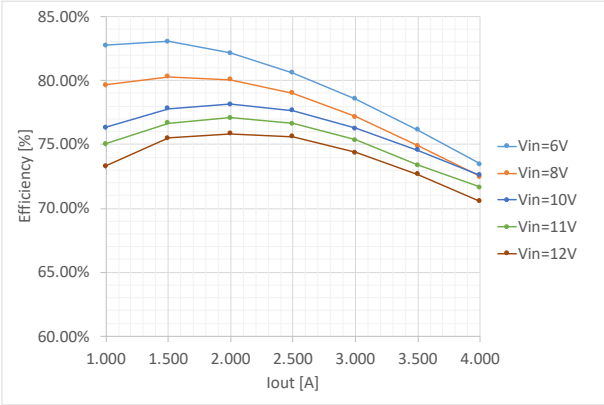


Figure 22: Module Efficiency for the Vout=2.5V version (with input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20°C.

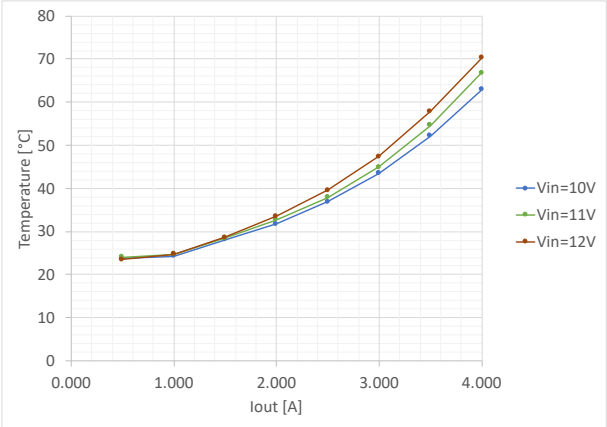


Figure 23: ASIC Increase of temperature for the Vout=2.5V version with different Vin and Iout, with the module in good thermal contact with a cooling plate at about 20°C.

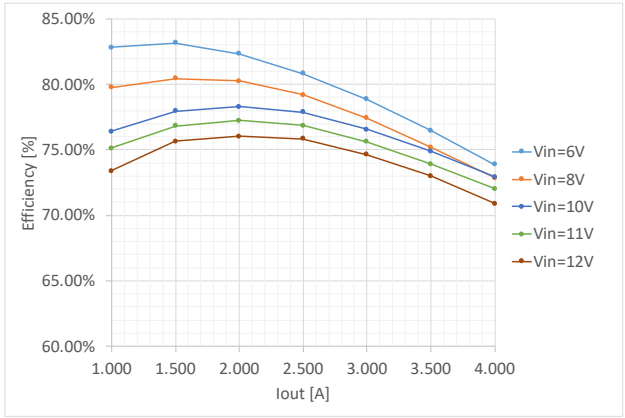


Figure 24: ASIC Efficiency for the Vout=2.5V version (without input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20°C.

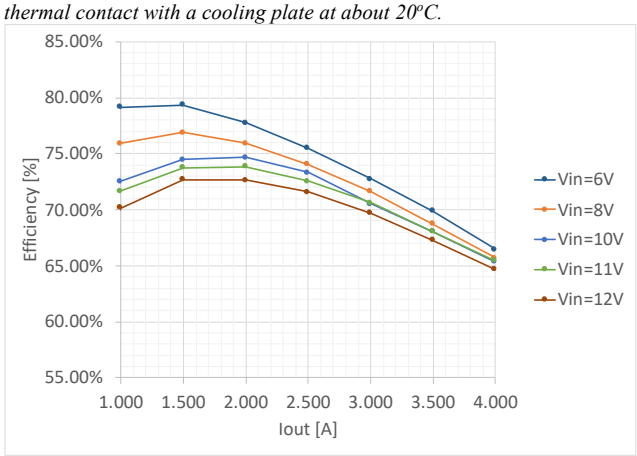


Figure 25: Module Efficiency for the Vout=1.5V version (with input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20°C.

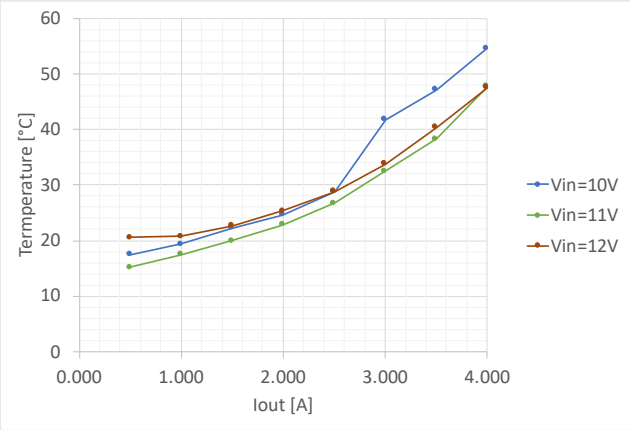


Figure 26: Increase of temperature for the Vout=1.5V version with Vin and Iout, with the module in good thermal contact with a cooling plate at about 20ºC.

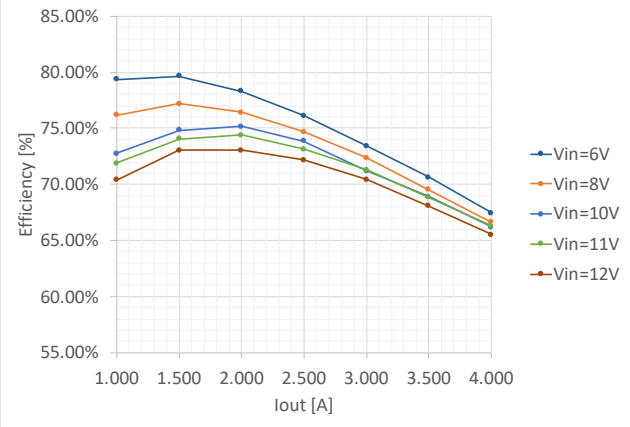


Figure 27: ASIC Efficiency for the Vout=1.5V version (without input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20ºC.

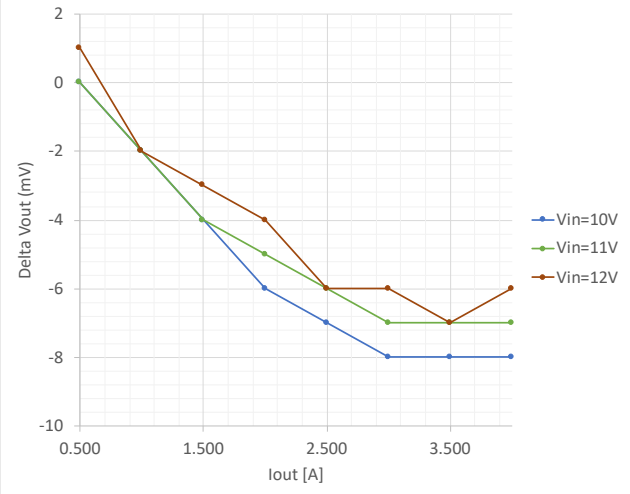


Figure 28: Module Load regulation for the Vout=1.5V version (with input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20ºC.

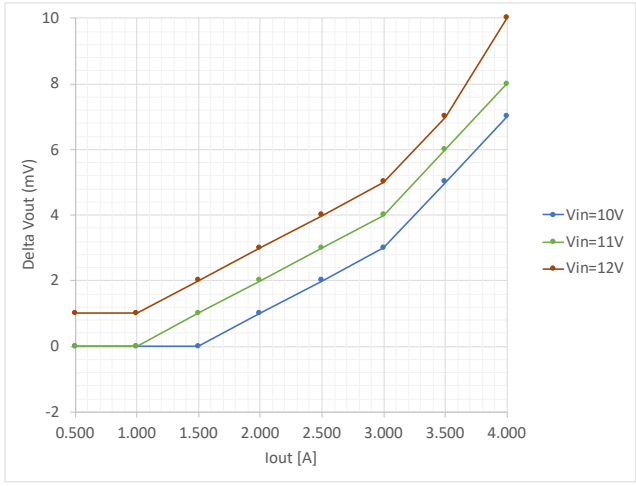


Figure 29: ASIC Load regulation for the Vout=1.5V version (without input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20ºC.

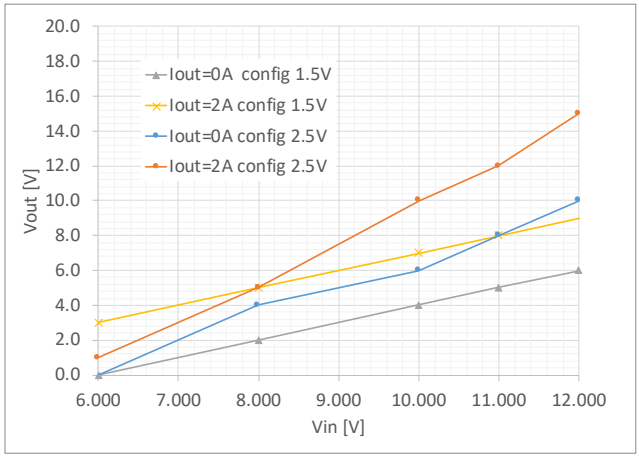


Figure 30: Module line regulation (with input+output π filters) and different Vin and Iout with the module in good thermal contact with a cooling plate at about 20ºC. The line regulation is not affected by the presence of the π filters

Package description

bPOL12V_V6 is packaged in a plastic Quad Flat No-Lead (QFN) package 5.0x5.0x0.9mm in size, with 32 pads and with an exposed pad to be soldered to the PCB for better thermal properties. The package is rated for a chip temperature increase of 27 to 31 ºC/W depending on the air flow. The suggested PCB layout for the integration of bPOL12V_V6 is shown in the following figure. The dimension of the signal pads is 0.25x0.5mm and the one of the central exposed thermal pad is 3.6x3.6mm. All distances are referred to the center of the signal or exposed thermal pads.

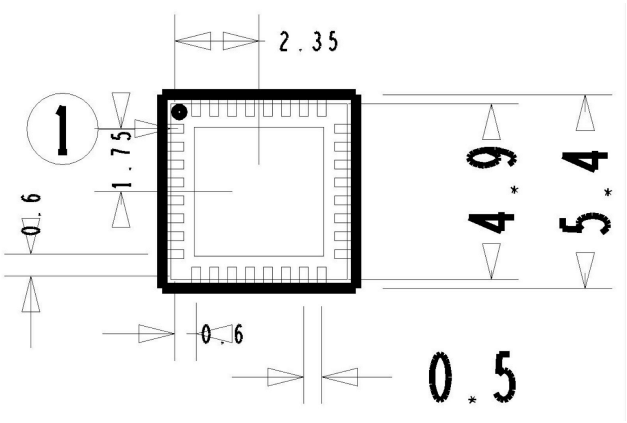


Figure 31: Suggested PCB layout for the integration of the bPOL12V_V6 QFN32 package.

Revision history

Revision	Date	Description
V1.0	Sept 2021	First release of the document, preliminary datasheet
V1.1	19/1/2022	Reviewed output filter for 2.5V configuration and updated VBGP=630mV
V1.2	Feb 2022	Corrected the value of Enable pulldown resistor to 15KOhm, not 1.5KOhm. Updated radiation tolerance plots and typical operation plots
V1.3	March 2022	Added SEE event waveforms
V1.4	May 2022	Added FEAST_MP_CLP like design link
V1.5	May 2022	Added max current for PTAT pin and updated DD results
V1.5.2	Aug 2022	Updated DD damage with neutron+proton DD tests
V1.6	Feb 2023	Updated DD tests with proton tests in IRRAD
V1.7	Nov 2023	Updated DD with Cyrce proton test in Aachen, updated BGP dispersion on the 140k dies production batch in August 2023
V1.8	Dec 2023	Updated Reliability results
V1.9	Jun 2024	Updated Reliability test from T. Gadek and stability informations