bPOL12V_V4

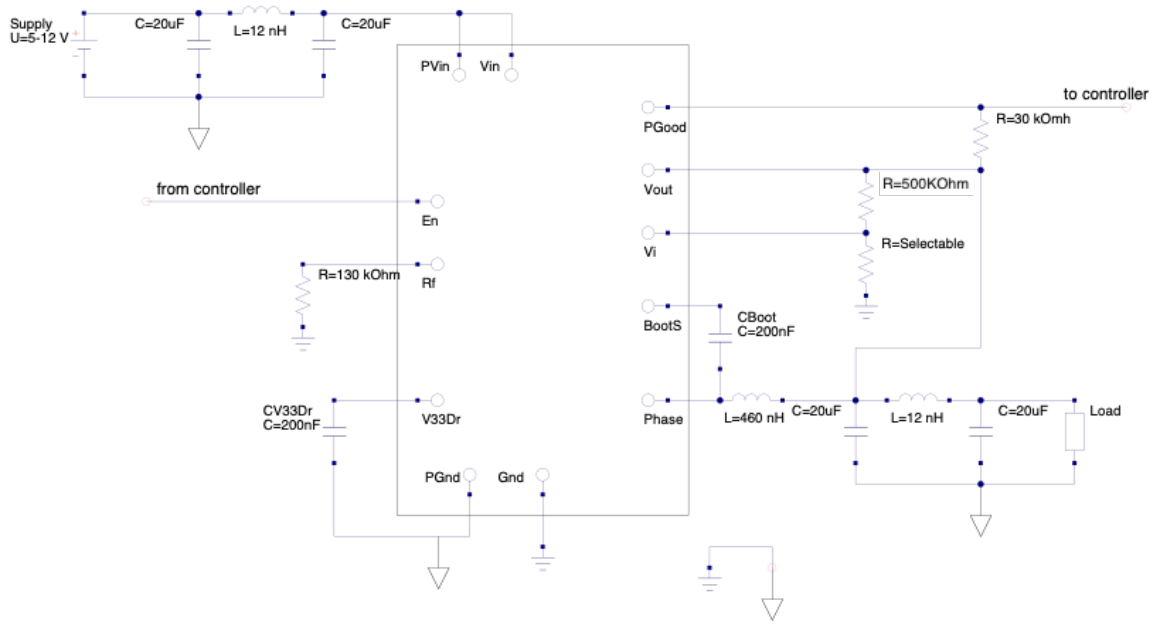
Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter

Features
- Input voltage range 5.5 to 10V
- Continuous 4A load capability
- Integrated Power N-channel MOSFETs
- Adjustable switching frequency 1-3MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Under-voltage lockout
- Over-Temperature protection
- Power Good output
- Enable Input
- Selectable Vout adjustment of +6.6%, -6.6% and -13.3%of the initial Vout value

Applications
Point Of Load in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

Description
bPOL12V_V4 is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the converter capable of continuous operation up to HL-LHC outer tracker radiation limit (50Mrad and 1e15 n/cm^2). bPOL12V_V4 has been designed for operation in a strong magnetic field in excess of 40,000 Gauss, and has been optimized for air-core inductors of 400-500nH: to be compatible with these small coil values, its switching operation is in the 1-3MHz range (1.5-2MHz for maximum efficiency).
The monolithic construction of bPOL12V_V4, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide POL regulation from a 5.5-10V supply rail. Its protection features include Over-Current, Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions. The chip temperature increase in the application can be monitored via a dedicated analog signal (PTAT).
Maximum suggested Vin voltage is 10V, reliability tests are on-going to check if Vin=11V is a reliable value.

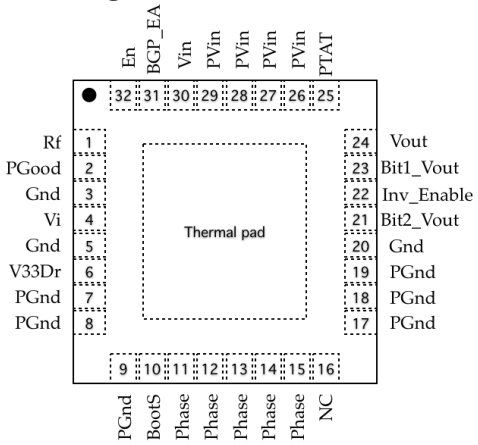
Typical application



Absolute Maximum Ratings

Power Input Voltage PVin……..…-0.3V to +10.0V
11V max PVin under reliability tests
Control Input Voltage Vin……..…..-0.3V to +10.0V
11V max Vin under reliability tests
Bootstrap Voltage BootS……..…..-0.3 to PVin+3.6V
Phase Voltage…..…0.3 V to Vin (DC), -2 to 12 V (AC, 10ns)
Phase to BootS Voltage…….…..…-0.3V to +3.6V
Driver Voltage, V33Dr..……..……...-0.3V to +3.6V
Feedback input Voltage of the E/A Vi…….……-0.3V to +3.6V
Frequency selector Rf……..…..-0.3V to +3.6V
Vout changer Bit1_vout and Bit2_Vout ……..…-0.3V to +3.6V
Reference voltage toggle Ref1V2……..……-0.3V to +3.6V
Converter Enable En ……..……..……..-0.3V to +3.6V
Power good PGood……..……..……-0.3V to +6.0V
Output Voltage Vout……..……..……-0.3V to +6.0V
Current in PGood pin (when PGood is negated)…..……50uA

Pin Configuration



Top view - 32-lead plastic QFN (5x5 mm)
Thermal pad must be soldered to PCB PGnd

Pin Function

Rf (Pin 1): Frequency Selector. A resistor placed between this Pin and the board GND determines the switching frequency of the converter as illustrated in the following table. The recommended range for best performance is 1.5-2 MHz. However, the switching frequency has to be adjusted, as a function of the selected inductor, to limit excessive peak-peak currents at every switching cycle that could affect long-term reliability. For 460nH inductor the suggested switching frequency is 1.8Mhz and for 220nH it is mandatory to have a switching frequency of at least 2.5Mhz. In other terms the product L*fs>550 MHz*nH. Maximum tested switching frequency is 3MHz.

Resistance (Ohm)	Frequency (MHz)
270K	1.03
200K	1.35
180K	1.48
160K	1.65
130K	1.99
100K	2.51
82K	2.98

PGood (Pin2): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 500uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout.

Gnd (Pin3, 5, 20): Ground of the control electronics of the converter. It must be connected to the PCB ground plane possibly in a location remote to the power current loop in the same plane.

Vi (Pin 4): Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 150kHz, but the DC regulation voltage Vout is selected by the addition of 2 resistors building a voltage divider between Vout and gnd. Vi is connected between the 2 resistors and the resulting voltage is compared to the internal reference voltage (about 0.6V). The resistor between Vout and Vi must have a value of 500KΩ, while the one between Vi and gnd is selectable (no resistor makes Vout = Vref).

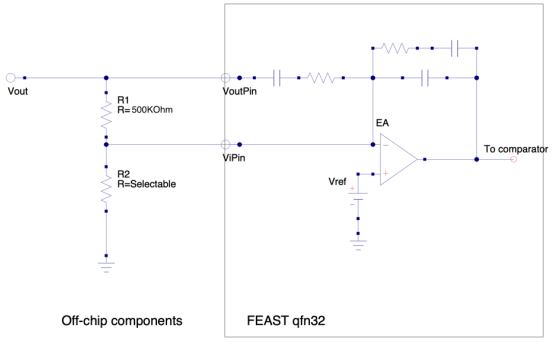


Figure 1: Configuring the output voltage.

V33Dr (Pin6): Voltage supply for the drivers of the power transistors. Although the regulator providing the 3.3V to the drivers is integrated, the large gate capacitance of the power switches requires a hefty charge storage element capable of providing quickly all the required transient current. This can not be achieved by on-chip capacitor, and an external capacitor of 220nF, positioned as close to the V33Dr pin as possible and directly connected to the PGnd (on the top PCB layer), is required.

PGnd (Pin 7, 8, 9, 17, 18, 19): Power Ground. This is the gnd of the power train and drivers, where large current transients are flowing. All PGnd pins must be connected to a large power plane under the qfn32, itself soldered to the Thermal Pad of the package, and connected to the PCB gnd plane by a large number of vias.

BootS (Pin 10): BootStrap capacitor voltage. bPOL12V_V4 uses 2 NMOS transistors in the power train, and the High Side (HS) switch requires a BootStrap circuit, which is embedded, for correct gate driving (the gate has to be connected to Phase for turn-off and to Phase+3.3V for turn-on). Given the large size of the HS power switch, an off-chip capacitor is required to provide the transient current to the HS drivers during switching. This capacitor, of 220nF, must be positioned between Phase and BootS pins, as close as possible to the qfn32 package.

Bit2_Vout (Pin 21): Pin to change the Value of Vout along with Pin23. If left floating the Vout is only determined by the voltage divider between Vout,Vi and GND.

Inv_Enable (Pin 22): Toggle of the polarity of the Enable pin. If this pin is connected to gnd, the polarity of the Enable pin is switched. It is recommended to leave this pin floating.

Bit2_Vout (Pin 23): Pin to change the Value of Vout along with Pin21. If left floating the Vout is only determined by the voltage divider between Vout,Vi and GND.

Vout (Pin 24): Regulated output voltage. This is an input pin bringing the Vout back to the converter's feedback circuit. It must be connected as specified in the description of Pin 4 (Vi).

PTAT (Pin 25): Proportional To Absolute Temperature provides and analog voltage whose variation with the chip junction T is linear with a slope of about 4.85mV/°C.

PVin (Pin 26, 27, 28, 29): Power Input Voltage. Input voltage of the power switches and drivers, where large current transients are flowing. Large input capacitances must be connected between this pin and PGnd as close to the package as possible (see board design recommendations later on).

Bgp_EA (Pin 31): The reference voltage to the Error Amplifier is buffered and made observable at this pin exclusively for test purposes. It is recommended to leave this pin floating.

Vin (Pin 30): Input Voltage for the control electronics of the converter. It is recommended to connect it to PVin close to the chip.

En (Pin 32): Enable input. bPOL12V_V4 is normally disabled and requires a voltage above 800mV applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V. There is an hysteresis, to switch off bPOL12V_V4 the Enable pin must be lower than 500mV. The polarity of the pin can be inverted by connecting Inv_Enable (Pin22) to gnd, in which case bPOL12V_V4 is enabled for applied voltages below 800mV. Note that an embedded 500 kΩ resistor pulls the voltage of the En pin to gnd.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - PVin, Vin	5.5	10	V
Output voltage - Vout	0.6	5	V
Conversion ratio - Vout/Vin	2	10	
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	4	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	10	W
Switching frequency	1.5	2.5	MHz
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	°C
Inductor value	220	500	nH
Enable voltage		3.3	V
Power Good voltage		3.3	V

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
PVin, Vin	Input voltage supply range	Converter operational, 11V still under test, recommended strongly 10V	5.5		10 (11 under reliability test)	V
Iin	Input current for control electronics (via Vin pin)	En pin low, converter disabled	-	8	-	mA

Iout *(note1)*	Output current	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	1	A
		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18ºC	-	-	4	A
Pout *(note1)*	Output power	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	2	W
		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18ºC	-	-	10	W
PWM						
DMax	Maximum Duty Cycle		-	97	-	%
DMin	Minimum Duty Cycle		-	0	-	%
Error Amplifier						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	20	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	10	-	V/µs
Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note2)*	-	5.5	-	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note2)*	-	5	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note2)*	-	800	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note2)*	-	500	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when bPOL12V_V4 is not powered)		-	10	-	kΩ
EnPullDownRes	Embedded Enable resistor to GND		-	500	-	kΩ
Protections						
OCPpk	Over Current Protection peak level	Vin=10V, Vout=1.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18ºC, *(note3)*	-	7.2	-	A
OCPavg	Over Current Protection average output current level	Vin=10V, Vout=1.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18ºC, *(note2, note4)* Vin=10V, Vout=2.5V, f=2.5MHz, L=220nH, Tcoolingpad≈18ºC, *(note2, note4)*	-	5.8 5.5		A
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level	-	120	-	ºC
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level	-	80	-	ºC
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=10V, Vout=2.5V, f=1.8MHz, L=410nH, Tcoolingpad≈18ºC, *(note2, note5)*		520		us
Power Good						
OV	Output Over Voltage PGood upper threshold			+6.5		%
UV	Output Under Voltage PGood lower threshold			-6.5		%
Proportional To Absolute Temperature signal						

PTAT	Analog output voltage	Converter disabled, environmental T sweep		4.85		mV/°C

Notes

Note 1: Max rated output current only allowed if max output power is not exceeded.
Note 2: Average value taken from measurements on 10 samples from the production run.
Note 3: This value has not been measured precisely and is reported as approximate indication of the peak current detection for OCP. The peak value does not have relevant dependence on Vin and Vout.
Note 4: The OCP uses a peak detector, hence the average output current for OCP detection depends on the input and output voltages. In particular, the OCP detection current for Vin=10V is not significantly different for Vout of 2.5 to 5V, whilst it increases by about 10% at 1.8V and even further at smaller output voltages.
Note 5: The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

Block Diagram

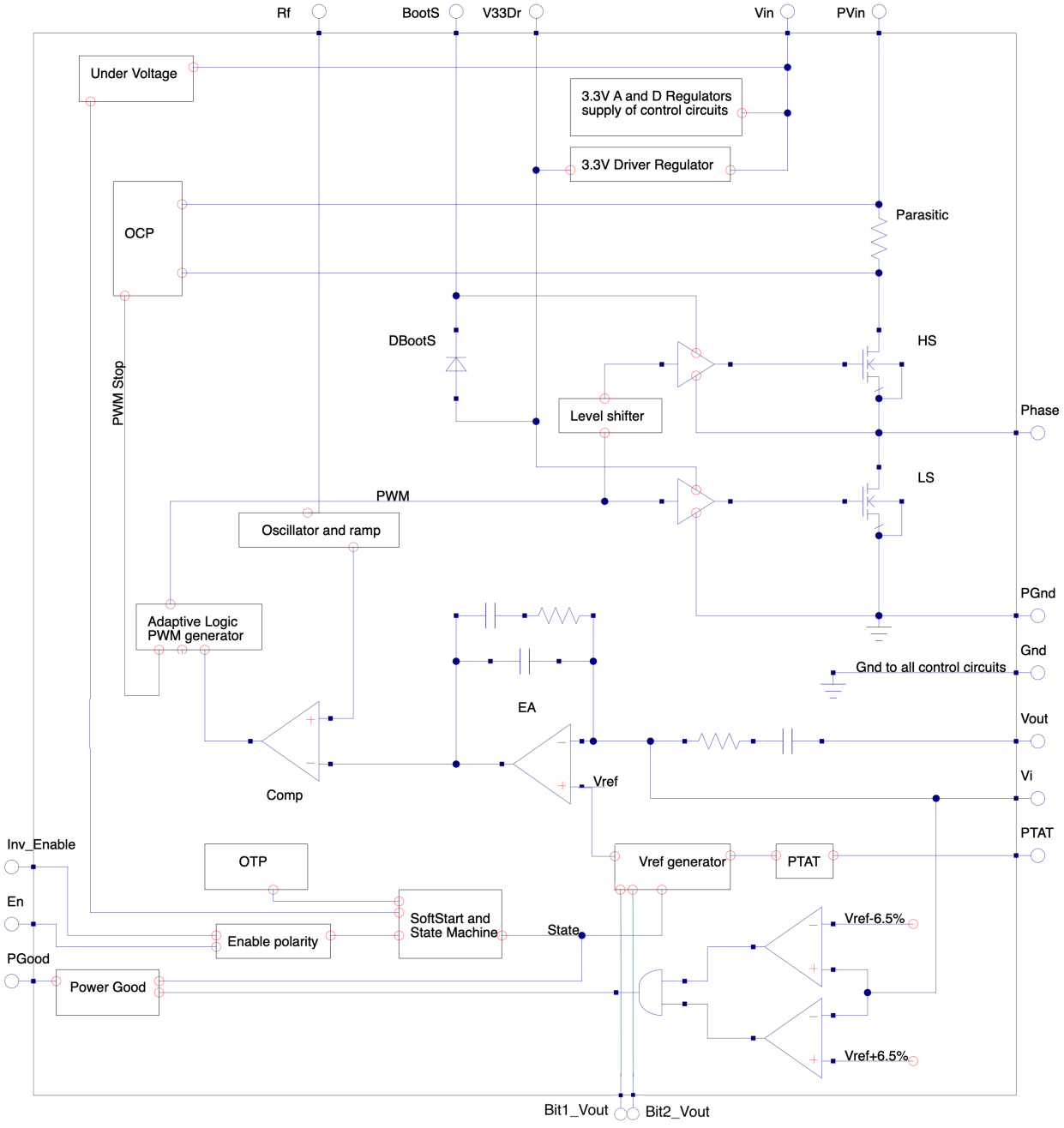


Figure 2: Block diagram of the bPOL12V_V4 ASIC.

Operation

bPOL12V_V4 is a DCDC converter designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace. The typical application at steady large load current with power provided from a remote supply (not from a battery) implies very relaxed requirements on quiescent current, while a fast feedback loop is at premium for some detectors where current consumption might have an instantaneous threefold increase.
bPOL12V_V4 has not been designed and tested for allowing large freedom in the choice of the external components (capacitors, inductors and resistors). The design of the board must follow the design that has been implemented with the module FEASTMP. Please contact dcdc.support@cern.ch for having more information on FEASTMP module and design files. Files are also available on EDMS at this address (https://edms.cern.ch/item/CERN-0000101871/0)

Output voltage selection
The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage (Vref) to the Error Amplifier. The production lot has been tested and the average value of the Vref is 615mV with st dev of 8mV.
The formula to calculate the proper R selectable for a wanted Vout Vout and given the Vref as above is:
Rsel=500KOhm*Vref/(Vout-Vref)
With the two pins Bit1_Vout and Bit2_Vout is it possible to slightly change the value of the Vout as follows:

Bit1_Vout,Bit2_Vout	Vout
0,0	nominal
0,1	-13.3%
1,0	-6.67%
1,1	+6.67%

Where 1 is the high value of Bit*_Vout. The pin threshold is 0.7V.
If the two Bit*_Vout pins are left floating the Vout is simply generated with the voltage divider.

Switching frequency
The switching frequency of the converter can be adjusted with one external resistor, which provides the bias current to the embedded oscillator. Although bPOL12V_V4 has been tested as functional over a wide range of frequency (1 to 3.5MHz), best performance is achieved in the range of 1.5-2MHz. At lower frequency, the peak-to-peak current in the small air-core inductor increases excessively and determines useless losses and possibly an early onset of the OCP. At higher frequency, driving losses increases dramatically and make the efficiency drop very sensibly. While usage at 1.5MHz allows top efficiency, 1.8MHz operation allows for reduced conductive noise and is preferred as default configuration. For some volume-limited application customers may use a 220nH inductor. It is anyway strongly suggested to use a higher value of inductance to decrease the peak-to-peak current that could affect long-term reliability. An inductance of 220nH requires a switching frequency of at least 2.5MHz.

Embedded linear regulators
While it can operate from a supply voltage of up to 10V, the control electronics in bPOL12V_V4 requires powering at 3.3V. A number of linear regulators are embedded to provide appropriate voltage to the drivers of the power transistors, to the bandgap and reference current generator, to the analog and to the digital circuitry. With the exception of the voltage regulation for the power transistors' drivers, all storage capacitors required for the regulators are on-chip and have been sized to ensure steady voltage even during large current surges.

Under-Voltage lockout
The embedded linear regulators need a sufficient level of over-voltage to provide stable 3.3V voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above about 5.5V (on rising Vin). This comparator has a hysteresis and bPOL12V_V4 is disabled again when, for falling Vin, the input voltage drops below about 5V.

Enabling bPOL12V_V4
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has not been asserted by applying a voltage above about 800mV. On Enable pin there is an hysteresis of 300mV, therefore bPOL12V_V4 will turn off when Enable pin's voltage is under 500mV. bPOL12V_V4 can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each bPOL12V_V4 providing regulated power to a different load). bPOL12V_V4 is disabled by default if the En pin is floating – an internal pull-down resistor of 500 kΩ keeps the voltage of the pin to gnd.
The polarity of the enable signal can however be inverted by connecting the Inv_Enable pin to gnd. In this case, the circuit is disabled when a voltage above 800mV is applied to the enable (En) pin and vice versa the circuit is enabled when a voltage below 500mV is applied; it is hence enabled by default if the En pin is floating – an internal pull-down resistor of 500 kΩ keeps the voltage of the pin to gnd.

Soft Start procedure
When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the EA, the output voltage reaching the nominal value in about 520us in the nominal configuration using the 0.6V bandgap (at the switching frequency of 1.8MHz, this time varying inverse linearly with frequency). Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that bPOL12V_V4 is correctly regulating the output voltage. For easy compatibility with almost any

CMOS logic level up to 3.3V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, in reset and when the output voltage is outside a ±6.5% window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 500uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PG pin is 3.6V.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip junction temperature and disables bPOL12V_V4 when it reaches about 120ºC. The OTP has a hysteresis of about 40ºC, hence the converter restarts (with SS) when the junction temperature decreases below 80ºC. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

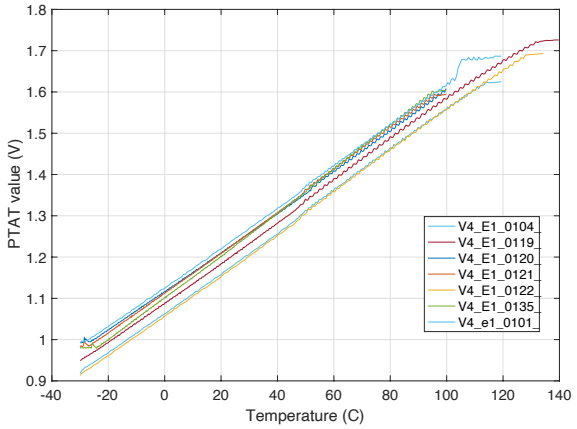
Over-Current Protection (OCP)
OCP is integrated as a real peak detector on the current flowing during each cycle in the HS transistor. Current sensing takes place on the parasitic resistance of metal lines bringing the input current from the input pads to the HS transistor. When the instantaneous current exceeds about 7.2 A, the PWM is reset and forces the HS to turn off. If the excessive load current condition persists, the on-time of the HS is not determined anymore by the feedback loop (which would require longer on-times to provide more output power) but by the OCP, and as a consequence the output voltage drops. This condition might endure as a steady state, PG being pulled to gnd if the output voltage drop exceeds 6.5% of the nominal. The peak current of 7.2 A translates in different average output current depending on the input and output voltage, frequency and inductor value.
For example, for a typical application Vin=10V, Vout=1.5V, fs=1.8Mhz. L=460nH the OCP average limited output current is around 5.8A. For Vin=10V, Vout=2.5V, fs=2.5Mhz. L=220nH the OCP average limited output current is around 5.5A.

Compensation network
The compensation network is fully integrated and determines a typical loop bandwidth of about 150kHz in the recommended operation environment (frequency, voltages, inductor, on-board passives). bPOL12V_V4 is hence capable of quickly adjusting the output voltage in case of output load transients.

Cooling
bPOL12V_V4 is specified for operation up to 10W output power. With an efficiency of 80% in case of large load current and not–cryogenic cooling, this translates in more than 2W lost in the converter (including the resistance of the inductor and of other passive components). Most of this power is burnt by bPOL12V_V4 itself and needs to be transferred to the cooling system efficiently. The chosen qfn32 package has an exposed cooling pad to which the IC is directly attached, and the pad must be soldered to the gnd plane of the PCB which itself must have a good thermal contact to the cooling system.

Proportional To Absolute Temperature (PTAT) voltage

The PTAT analog signal can be used to monitor the T increase of the bPOL12V_V4 ASIC during operation, in particular to verify that the cooling is appropriate. The absolute value of the PTAT voltage at a given T has a wide sample-to-sample variability. However, the PTAT increase with respect to T is very close to a straight line with slope 4.85 mV/ºC. This has been verified on 7 samples: although the PTAT value at the same T could vary by 200mV, all samples had a linear dependence between **Δ**PTAT and **Δ**T, with a very similar slope (averaging 8.5). This linear relation is shown for one of the measured samples in the figure below.



Typical operation waveforms

Full characterization of the bPOL12V_V4 ASIC has been done on prototypes mounted on prototype DCDC modules. Plots will be available soon.

Package description

bPOL12V_V4 is packaged in a plastic Quad Flat No-Lead (QFN) package 5.0x5.0x0.9mm in size, with 32 pads and with an exposed pad to be soldered to the PCB for better thermal properties. The package is rated for a chip temperature increase of 27 to 31 ^{o}C/W depending on the air flow. The suggested PCB layout for the integration of bPOL12V_V4 is shown in the following figure. The dimension of the signal pads is 0.25x0.5mm and the one of the central exposed thermal pad is 3.6x3.6mm. All distances are referred to the center of the signal or exposed thermal pads.

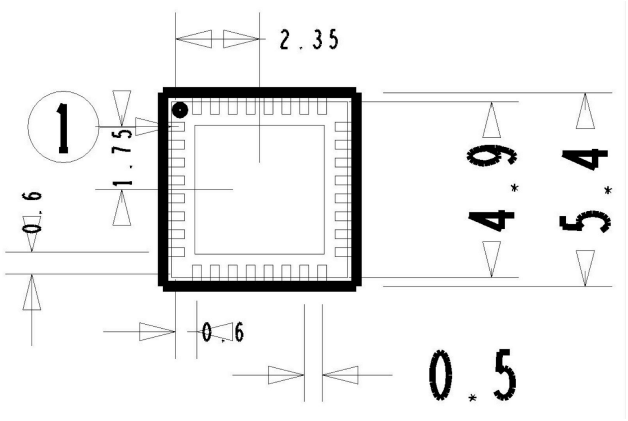


Figure 3: Suggested PCB layout for the integration of the bPOL12V_V4 QFN32 package.

Revision history

Revision	Date	Description
0	April 2020	First release of the document, preliminary datasheet