bPOL12V_V6 Layout guidelines

Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter

Introduction

This document is an annex of the bPOL12V_V6 datasheet. The main PCB layout considerations in order to improve performance and reliability are discussed.

bPOL12V is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment.

The monolithic construction of bPOL12V, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide point of load (POL) regulation.

Given the used technology, the power devices could experience voltage stress close to or exceeding the recommended values depending on the parasitic elements external to the bPOL12V package. Therefore, care should be taken when designing the PCB and selecting the input filter components in order to ensure a reliable and continuous operation of the converter.

Input power loop impedance

Figure 1 shows a simplified schematic of a buck converter power stage, with the input loop most relevant parasitic inductances. The current in the input loop has a trapezoidal shape, with large di/dt on the switching instants. This current shape could generate large voltage spikes due to the parasitic inductance on the input loop, composed by the inductance of the PCB and the internal wire bonds (Llk1 and Llk2) and the equivalent series inductance of the input capacitor (ESL). The peak voltage across the switches should not rise above 14V, which leaves a very small margin when operating with input voltages in the range of Vin=10V to Vin=12V.

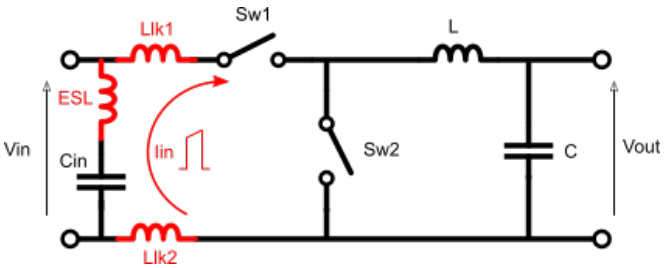
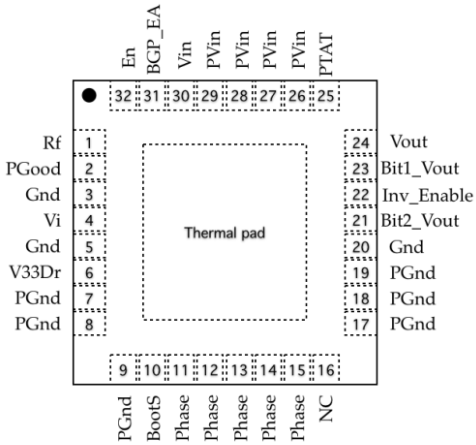


Figure 1: Buck converter simplified schematic

In order to keep the power MOSFETs working in a safe condition, the total value of the parasitic inductance (including PCB, capacitor and wire bonds) should be less than 700pH for Vin=11V, and less than 450pH for Vin=12V.

Layout recommendations

bPOL12V is provided on a 32-lead plastic QFN package, shown on Fig. 2. The input power loop is formed between PVin pins (26-29) and PGnd pins (7-9 and 17-19), across the closest input capacitor.



Top view - 32-lead plastic QFN (5x5 mm)
Thermal pad must be soldered to PCB PGnd

Figure 2: bPOL12V pin configuration

A recommended layout for bPOL12V is shown on Fig. 3 and Fig. 4. This layout aims to minimize the loop area by generating a low-profile current path using a multilayer PCB, and a low ESL capacitor as close as possible to the input power pins. The top layer of the PCB, shown on Fig. 5, is used to route the input voltage to the PVin pins, and to allocate the thermal connection and GND vias. Furthermore, the first inner layer is used as a return path to connect the PGnd pins with the GND pin of the input capacitor.

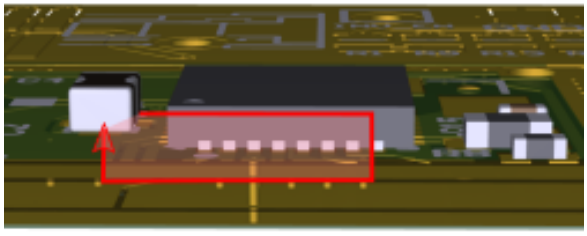


Figure 3: Power loop side view

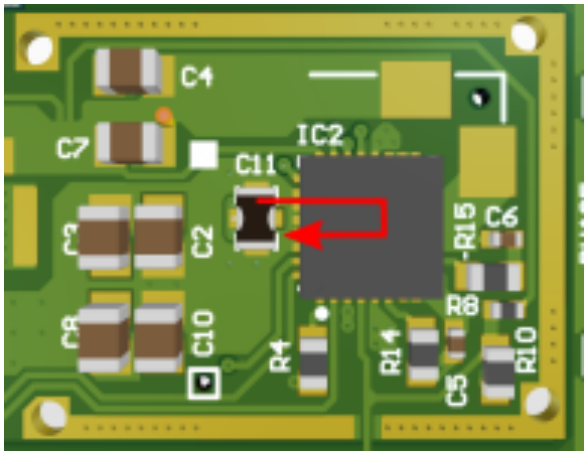


Figure 4: Power loop top view

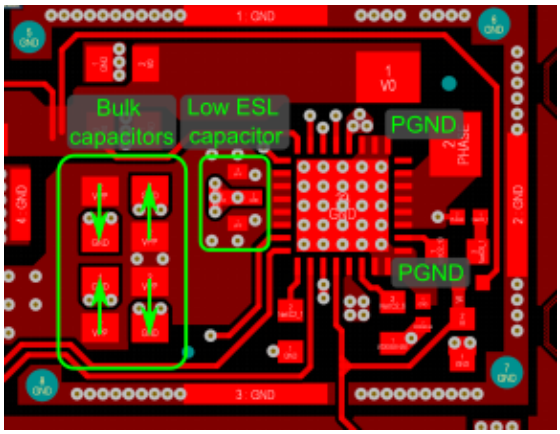


Figure 5: Top layer view.

As it can be noticed, in order to optimize the previously described layout, both the layer stackup of the PCB and the input capacitor need to be carefully selected.

Concerning the input capacitor, the recommended part number is NFM21PC104R1E3 (NFM series from MURATA), which provides very low equivalent series inductance in a 0805 (2012M) package. However, if this type of capacitor cannot be used due to size or thickness constraints in the final application, a low ESL 0306 such as LLL03TR61E223KE01 could also be used. In addition to the high frequency capacitor, at least 20uF of bulk capacitance is required to ensure stability and reduce the voltage and current ripples at the switching frequency. In order to improve the dynamic response, several parallel multilayer ceramic capacitors are recommended, placed in a 180º rotation to provide a negative coupling coefficient [1].

Regarding the layer stackup, the thickness of the dielectric between top layer and the first inner layer should be reduced as much as possible. Even though the PCB is simple enough to be routed in only 2 layers, it is recommended to use at least 4 layers in order to reduce as much as possible the distance between top and the first inner layer (vertical loop height), while providing mechanical stability using the core dielectric. An example of a standard process providing good results is using a 4 layers PCB with a 0.5mm core (e.g., VT-447) and a 60um prepreg (e.g., VT-447 1080 RC66) as dielectric between external and internal layers.

The complete reference design files can be found in https://edms.cern.ch/project/EDA-04466.

Simulated performance

In order to better illustrate the impact of the layout in the parasitics of the input power loop, the PCB was simulated using ANSYS Siwave. This tool allows to extract the inductance of the loop by combining the SPICE model of the components with the physical structure of the PCB.

Two different situations have been evaluated, a two-layer PCB using a 300um dielectric (such as the previous module called FEASTMP) and the layout suggested in this document. In both cases, the wire bonds have been considered and are of equal length and shape. The results are shown on Fig. 6, where it can be seen that, by using the recommended layout, the parasitic inductance is reduced from 1.2nH to 330pH, which yields 2V reduction in the amplitude of the overvoltage spike.

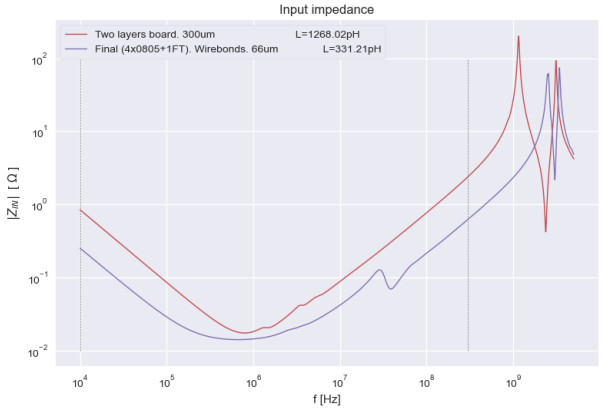


Figure 6: Input impedance

References

[1] Fuentes, C., Allongue, B., Blanchot, G., Faccio, F., Michelis, S., Orlandi, S., Pontt, J., Rodriguez, J., & Kayal, M. (2011). Optimization of DC-DC Converters for Improved Electromagnetic Compatibility With High Energy Physics Front-End Electronics. *IEEE Transactions on Nuclear Science*, *58*(4), 2024–2031. https://doi.org/10.1109/TNS.2011.2159395

Revision history

Revision	Date	Description
0	Sep 2021	First release of the document