Production testing of FEASTMP modules

This document describes the approach used to verify the functionality of all production samples of FEASTMP. A dedicated measurement setup has been developed to this purpose and is maintained at CERN-PH-ESE. A PC controls a series of instruments and runs a pre-defined sequence of measurements on each module; it then compares the extracted results with pre-defined acceptance criteria. All the extracted parameters have to fall inside the acceptance window for the module to be labeled as good and distributed to the users.

The test system

The production testing aims at discarding faulty FEASTMP modules and preventing their distribution to users. It is hence a screening test to be run on all production samples; therefore it has to be simple, fully automatized and rapid.

The test system comprises:

- a power supply providing the input voltage
- a programmable electronic load that determines and measures the output current
- an Amp-meter and a Volt-meter to measure precisely the input current and all test voltages – the Volt-meter is connected to the appropriate line via a switching box)
- a custom test box where the FEASTMP module to be tested is plugged and providing electrical and thermal interfaces for the test. This includes a 'receiving board' where the module is plugged for the test and where all voltages are measured
- a cooling system based on a peltier element, a temperature sensor and a microcontroller, keeping the temperature of the cooling plate for the module at 18°C
- a bar-code scanner to read the labels uniquely identifying each FEASTMP sample
- a dedicated PC that runs all the control software performing several tasks: the user interface, the control of the instruments, the elaboration of the data and the comparison of the extracted parameters with the acceptance criteria, the formatting for insertion in a database.

An image of the test system is shown in Figure 1, while a block diagram in Figure 2.

After a unique identifier has been attached to each module with a machine-readable label (bar-code), the test sequence starts by plugging the module to the connector in the test box, then reading the identifier with the bar-code scanner, then pressing a 'start test' button on the PC. The measurement sequence starts and takes about 40s to complete. At the end of the test, a display clearly indicates if the module is accepted or rejected, and all the data are registered in a database. The test can hence be run by an unqualified operator.

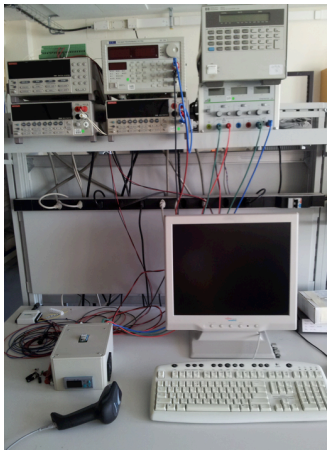

Figure 1: The production test system.

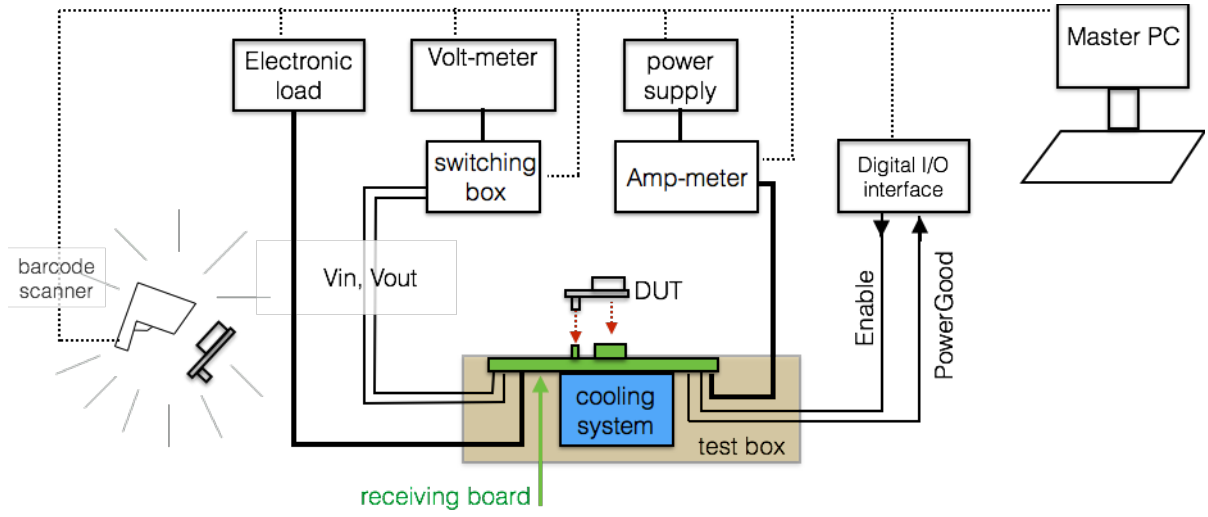

Figure 2: block diagram of the test system

Measurement sequence

A sequence of 10 measurements is executed during the production testing of all DCDC modules, each at a different Input Voltage or Output Current. For each measurement, the input and output voltages and currents are recorded. Table 1 lists the specific conditions for the 10 measurements.
The correct functionality of the enable is also verified: a switch selects the voltage applied to the Enable pin (2.5V or 0V) while the voltages at the output and at the Power Good pin are monitored. This also allows verification of the functionality of the Power Good (the Power Good line should be pulled to ground by the module when the converter is disabled).

Vin (V)	Iout (A)
7	1, 2, 4
10	0, 1, 2, 4
12	1, 2, 4

Table 1: Matrix of input voltage and output current conditions for the 10 measurements performed during the test sequence

Acceptance criteria

The acceptance criteria have been defined to ensure that the basic features of the module in the list below are correct:

- the module turns on and off on command (enable)
- the Power Good flag correctly reflects the status of the converter
- the module is providing the correct output voltage with and without load
- the conversion efficiency is within expectations.

The comparison with the criteria requires some data handling, which is performed automatically by the software. In order to reduce the test time for each module, only the measurements at an input voltage of 10V are used for the acceptance. Table 2 details the parameters that are extracted from the measurements and compared to pre-defined values. Table 3 reports the 'reference' parameters, those that are used for the comparison and that constitute hence the acceptance criteria.

Acceptance criteria for the output voltage (Vout)

The output voltage is determined by the on-chip bandgap reference voltage (no trimming possible) and by the ratio between 2 SMD resistors (1% precision) mounted on the FEASTMP module. This leads to dispersion in the output voltage of the converters. On the basis of the available data on a large number of modules, the dispersion around the average is below ±3.7%.
As shown in the FEASTMP datasheet, the parasitic resistances on the output current path (filter inductor, power connector) determine a current-dependent drop in the output voltage of the module, measured on the receiving board. The available data indicate that the drop at 2A is about 25mV (hence Vout@0A ≈ Vout @2A + 25mV). Since in the application the converters will provide an output current, the target output voltage for each module is obtained adding 25mV to the required voltage, so that they will regulate the required voltage when providing 2A load current.
The target voltage drives the choice of the SMD resistors, but this requires the knowledge of the average value of the bandgap reference voltage. From this average, the SMD resistors are chosen to yield the best voltage match for the target (SMD are only available in discrete values), which constitutes the nominal voltage of the modules. The acceptance limits VoutMin and VoutMax are calculated at 3.7% below or above this nominal voltage.

Parameter	Detail
VoutZero	Output voltage for zero load current (compared to limits VoutMin and VoutMax)
Drop1	Vout drop for 1A load: Vout@1A - Vout@0A
Drop2	Vout drop for 2A load: Vout@2A - Vout@0A
Eff1	Efficiency for 1A load
Eff2	Efficiency for 2A load
Pgood	Power Good flag ok
enable	Enable control ok

Table 2: Parameters used for the acceptance of the FEASTMP modules. These are all measured for an input voltage of 10V.

Required Vout (V)	Nominal Vout (V)	VoutMin (V)	VoutMax (V)	Drop1Max (mV)	Drop2Max (mV)	Eff1Min (%)	Eff2Min (%)
1	1.025	0.987	1.063	25	35	65	66
1.2	1.221	1.176	1.266	25	35	68	69
1.44	1.467	1.413	1.521	25	35	72	73
1.5	1.532	1.475	1.589	25	35	72	73
1.55	1.576	1.517	1.634	25	35	72	73
1.8	1.811	1.744	1.878	25	35	74	75
2	2.032	1.957	2.107	25	35	76	77
2.5	2.511	2.418	2.604	25	35	80	81
2.6	2.613	2.516	2.710	25	35	80	81
2.66	2.704	2.604	2.804	25	35	80	81
2.8	2.836	2.731	2.941	25	35	80	81
3	3.025	2.913	3.137	30	35	81	82
3.3	3.332	3.208	3.455	30	35	81	82
3.8	3.828	3.686	3.969	35	35	82	83
5	5.004	4.819	5.190	40	35	85	86

Table 3: Acceptance criteria for the different parameters extracted from the systematic measurements of each FEASTMP The nominal Vout should correspond to the average output voltage of a large number of modules at 0A load. Note: VoutMin and VoutMax are different for the first assembly run (summer 2014) as detailed in the appendix below.

Appendix: Acceptance criteria for the first assembly lot

The acceptance criteria for VoutMin and VoutMax specified in Table 3 are not valid for samples from the first assembly run (summer 2014) because the average value of the bandgap with the converter turned on was not precisely known at the time of the assembly. In particular, the value of the bandgap was under-estimated by 5-6 mV and this resulted in modules providing a slightly larger voltage than the target. The VoutMin and VoutMax have hence been increased in order for the acceptance window to be centered around the resulting average Vout. The used values are listed in Table 4. The limits for the Types 1V and 2.66V were unchanged because by chance the small number of samples in these 2 voltages were all passing the criteria in Table 3.

Required Vout	VoutMin	VoutMax		Required Vout	VoutMin	VoutMax
1	0.990	1.060		2.5	2.456	2.645
1.2	1.188	1.279		2.66	2.590	2.780
1.44	1.431	1.541		3	2.965	3.193
1.5	1.473	1.586		3.3	3.215	3.462
1.8	1.770	1.906		5	4.939	5.318
2	1.953	2.104				

Table 4: Modified acceptance criteria for the first FEASTMP assembly run (summer 2014).

Revision history

Revision	Date	Description
1.0	Sept. 2014	First release of the document.