FEASTMP

Radiation and magnetic field tolerant 10W DC/DC converter module

Features
- Input voltage range 5 to 12V
- Continuous 4A load capability (dependent on output power level, limited to 10W)
- Available in different output voltage versions from 0.9 to 5V (minimum achievable with the FEAST ASIC 0.6V)
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Input under-voltage lockup
- Over-Temperature protection
- Power Good output
- Enable Input
- Fast acting fuse in series at the input of the module to protect the line in case of module failure
- EMC: conducted noise compatible with Class-B CISPR11 requirements in most conditions of Vin and Iout
- Shielded to make it compatible with operation in close proximity (1cm) to sensitive detector systems
- Radiation tolerant: TID up to >200Mrad(Si), displacement damage up to $5x10^{14}n/cm^2$ (1MeV-equivalent), absence of significant SEEs up to $>65MeVcm^2mg^{-1}$ (only short SETs smaller than 20% of the nominal Vout are observed)
- Magnetic field tolerance in excess of 40,000 Gauss

Applications
- Point Of Load (POL) converter for electronics systems of HEP detectors, or wherever radiation and magnetic field tolerance is required.

Description

FEASTMP is a full DC/DC converter module built around the FEAST2 DC/DC radiation-tolerant ASIC to the purpose of providing HEP experiments with converter modules in system tests and detector upgrades.

The FEAST2 ASIC has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the converter capable of continuous operation up to more than 200Mrad(Si) total ionizing dose and an integrated particle fluence of $5x10^{14}n/cm^2$ (1MeV-equivalent). Single Event Effects resilience has been tested at a Heavy Ion irradiation facility, showing that the circuit is free of resets or other significant SEE up to an LET of $65MeVcm^2mg^{-1}$ (no data available for higher LETs). Only Single Event Transients (SET) are observed with amplitude below 20% of the nominal output voltage, and of duration typically smaller than 2us.

FEASTMP has been designed for operation in a strong magnetic field in excess of 40,000 Gauss: its coils (the main energy storage element of 460nH and 2 inductors in the input-output filters) are air-core. Given the small inductance of the main coil, the switching frequency is set at about 1.8MHz.

The monolithic construction of FEAST2, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide POL regulation from a 5-12V supply rail. Its protection features include Over-Current, Over-Temperature and Under-Voltage to improve system-level security in the event of fault conditions.

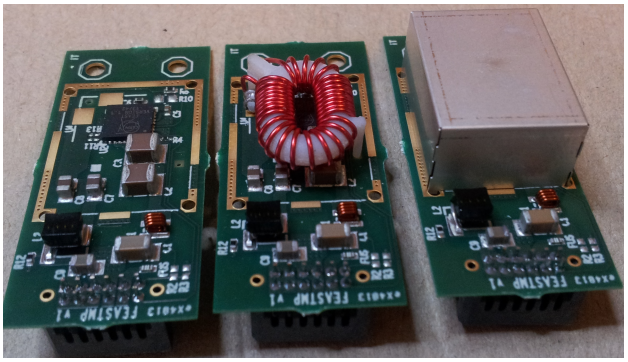


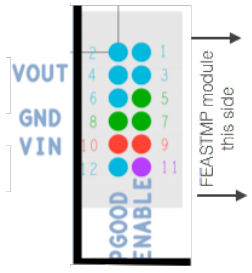
Figure 1: View of the FEASTMP module fully assembled (right), with shield removed (center) and with main inductor removed (left).

Absolute Maximum Ratings

Power Input Voltage, PVin……..……-0.3V to +12.3V
Converter Enable, En ……..……..-0.3V to +3.6V
Power good, PGood……..……-0.3V to +5.5V
Output Voltage, Vout……-0.3V to +5.5V
Current in PGood pin (when PGood is negated)…….50uA

Pin Configuration

Pin Number	Function
12	PGood
11	En
1,2,3,4,6	Vout
5,7,8	Gnd
9,10	Vin



Pin Function

PGood (Pin12): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider if the CMOS logic level required for the PGood signal is below Vout. The value of the pull-up resistor determines the current in the open-drain NMOS, which has to be limited below 50uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout. In case the pull-up resistor is not connected to Vout but to another available voltage supply, it is possible that the PG signal is asserted when the converter is not properly powered (in this case, there is no valid voltage on-chip to bias the gate of the open-drain NMOS, which can hence not drive the PG signal to gnd).

En (Pin11): Enable input (max voltage 3.3V). FEASTMP is normally disabled and requires a voltage above 850mV applied to this pin to be enabled and start operation. This voltage value has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V.

Gnd (Pin 5, 7, 8): Ground of the converter.

Vout (Pin 1, 2, 3, 4, 6): Regulated output voltage.

Vin (Pin 9, 10): Power Input Voltage.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - PVin, Vin	5	12	V
Output voltage - Vout	0.9	5	V
Conversion ratio - Vout/Vin	2	10	
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	4	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	10	W
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	20	^{o}C
Enable voltage		3.3	V
Power Good voltage		5	V

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
PVin, Vin	Input voltage supply range	Converter operational	5	-	12	V
Iout *(note1)*	Output current	Vin=10V, Vout=2.5V, PCB in air	-	-	1	A
		Vin=10V, Vout=2.5V, good thermal contact with cooling plate at 18^{o}C or below	-	-	4	A
Pout *(note1)*	Output power	Vin=10V, Vout=2.5V, PCB in air	-	-	2	W
		Vin=10V, Vout=2.5V, good thermal contact with cooling plate at 18^{o}C or below	-	-	10	W
Input Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note2)*	-	4.79	-	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note2)*	-	4.52	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note2)*	-	815	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note2)*	-	730	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when FEAST is not powered)		-	10	-	kΩ

Protections						
OCPpk	Over Current Protection peak level	Vin=10V, Vout=2.5V, Tcoolingpad≈18°C, *(note3)*	-	6	-	A
OCPavg	Over Current Protection average output current level	Vin=10V, Vout=2.5V, Tcoolingpad≈18°C, *(note2, note4)*	-	4.8		A
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level, *(note5)*	-	103	-	°C
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level, *(note5)*	-	73	-	°C
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=10V, Vout=2.5V, Tcoolingpad≈18°C, *(note2, note6)*	-	440	-	us

Notes

Note 1: Max rated output current only allowed if max output power is not exceeded.
Note 2: Average value taken from measurements on 10 samples using FEAST2 chips from the production run.
Note 3: This cannot be measured on production boards (no place to put the current probe to measure the current in the inductor), so this value is estimated from measurements on test modules. The peak value does not have relevant dependence on Vin and Vout.
Note 4: The OCP uses a peak detector, hence the average output current for OCP detection depends on the input and output voltages. In particular, the OCP detection current for Vin=10V is not significantly different for Vout of 2.5-5V, whilst it increases by about 10% at 1.8V and even further at smaller output voltages.
Note 5: The threshold temperature for OTP is approximate, since it is not measured on-chip (no junction T available). Modules regulating 2.5V with no load were put in good thermal contact with a thermal chuck, and T was increased. The temperature of the chuck when the FEASTMP module turned off (and back on) was taken as threshold.
Note 6: The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

Operation

Switching frequency
The switching frequency of the converter is adjusted on-board with one resistor, which provides the bias current to the on-chip oscillator. The nominal frequency is set to 1.8MHz by default.

Input Under-Voltage lockout
The on-chip linear regulators providing the appropriate 3.3V to the control electronics need a sufficient level of over-voltage for proper operation. To prevent faulty operation because of lack of appropriate supply to the control electronics, a 2-level under-voltage lockout system is implemented. A first comparator only authorizes the linear regulators to turn on when Vin is above 4.3V (on rising Vin). This comparator has an hysteresis and turns off the regulators on falling Vin at 3.6V. An asserted output of this comparator enables on-chip power to be distributed but is not sufficient for the converter to be functional. A second comparator output needs to be asserted to enable the module, and this happens at an input voltage of about 4.8V (on rising Vin). This comparator also has an hysteresis and FEASTMP is disabled again when, for falling Vin, the input voltage drops below about 4.5V.

Enabling FEASTMP
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has been asserted by applying a voltage above 850mV. FEASTMP can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each FEASTMP providing regulated power to a different load).

Soft Start procedure
When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the on-chip reference voltage of the EA, the output voltage reaching the nominal value in about 440us. Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that FEAST is not in a faulty state. For easy compatibility with almost any CMOS logic level, this output is an open drain (of an NMOS High-Voltage transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, during reset and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout. In the absence of Vin, or in under-voltage lockout (first level), power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 50uA, so an appropriate pull-up network has to be selected.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip junction temperature and disables FEAST when it reaches about 103°C (the OTP temperatures are not precisely measured since T is not measured on the FEASTMP board itself). The OTP has a hysteresis of about

30°C, hence the converter restarts (with SS) when the junction temperature decreases below 73°C. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

Over-Current Protection (OCP)
OCP is integrated as a real peak detector on the current flowing during each cycle from Vin: when the instantaneous current exceeds about 6A, the OCP sets in. As a consequence, Vout drops below nominal regulation value. This condition might endure as a steady state, PG being pulled to gnd. The peak current of 6A translates in different average output current depending on the input and output voltage, but it is typically around 4.8A.

Line protection in case of module failure
In the typical configuration in detector systems several FEASTMP will share the same input voltage line. In case of any failure of one of the modules, the line should be protected to limit the propagation of the effects of the failure. A fast acting 0402 fuse is embedded in series to the input line to this purpose: if the failure is a short to gnd, the current eventually burns the fuse and isolates the module from the line. The chosen fuse is rated to 3A to be compatible with the maximum input current in the specification range of FEASTMP. It is a fast acting device from Littelfuse (0435003.KR). The following chart has been extracted from the component's datasheet and provides the average time for the fuse to burn.

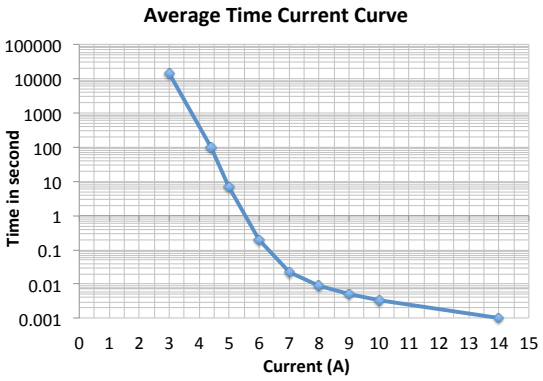


Figure 2: Average time for the fuse to burn and open the circuit.

Compensation network
The compensation network is fully integrated on-chip and determines a typical loop bandwidth of about 150kHz. FEASTMP is hence capable of quickly adjusting the output voltage in case of output load transients.

Cooling
FEASTMP is specified for operation up to 10W output power. With an efficiency of 80% in case of large load current and not–cryogenic cooling, this translates in more than 2W lost in the converter (including the resistance of the inductor and of other passive components). Most of this power is burnt by FEAST itself and needs to be transferred to the cooling system efficiently. The chosen QFN32 package has an exposed cooling pad to which the IC is directly attached, and the pad is soldered to the gnd plane of the FEASTMP module. This plane is exposed as a large thermal pad in the bottom side, which must have a good thermal contact to the cooling system.

Output voltage variation
The output voltage is set by the choice of one of the two SMD resistors in the regulation voltage loop at the time of assembling the modules. The choice of this resistor is guided by the average value of the bandgap voltage (Vbg_{avg}) measured on wafers of the FEAST2 ASIC (40 test points per wafer). The bandgap voltage generator is not trimmed, so the distribution of the voltage over the samples is rather large, estimated at about ±2.8% (3 sigma) from the on-wafer tests. The external resistors in the voltage loop are 1% components and add another error to the output voltage. Overall, the distribution of values for a large number of samples could well have tails exceeding ±4%. To limit the accepted variation in Vout, the production test procedure has an acceptance window of ±3.7% around the nominal.
It is important to specify what this nominal voltage is. The procedure to calculate it is the following:

- Definition of the desired output voltage (example: 1.2V)
- Increase of this voltage by 25mV (example: 1.225V). This is done to take into account that the voltage seen by the user of the module decreases with the load current, as shown in the typical operation waveforms below. The decrease is due to the parasitic resistance of the inductor in the output filter and of the power connector. Measured on-module before the filter's inductor, the variation of Vout is typically below 8mV over the full load range of 0-4A. To partially compensate for this drop and since in most applications the converter is actually providing an output current, the target output voltage at 0A load is increased by 25mV so that the converter will better meet the Vout specification at 2A of load. The 25mV value is chosen on the basis of the test of the first production lot of 1000 modules.
- From the target voltage (1.225V in the example) and the average bandgap voltage Vbg_{avg} we calculate the ideal resistor for the feedback voltage loop. Since SMD resistors are available for pre-determined values only, and we use 1% tolerance components, the resistor providing the best match to the target voltage is chosen. This determines the nominal voltage of the converter: for a large number of samples, the average measured Vout should be around this value.

More information about the values for each lot can be found in the document describing the production test methodology.
It should also be noted that, in case of poor cooling, the output voltage could sensibly increase at large load current because of the increase of the ASIC temperature – to which the bandgap voltage is sensitive.

Module size, footprint, and stack height

The outline of the module, seen from above, is shown in the following image together with all relevant sizes. The 12-pin power connector is located to the left, while two 2.1mm diameter holes are located to the right giving the possibility to screw the module to a cooling plate to ensure efficient cooling. The highlighted rectangle in the middle of the module represents the shield, which is 8mm high, under which the ASIC, the main inductor and most of the other passives are arranged.
When mated, the connector height (from the motherboard to which the module is connected) is 5.97mm. Adding the 0.4mm thickness of the PCB and the 8 mm height of the shield, the full stack height is just short of 15mm.

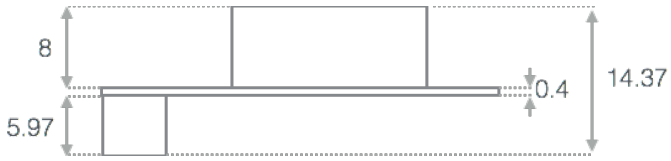


Figure 3: Side view of the FEASTMP module with mechanical dimensions.

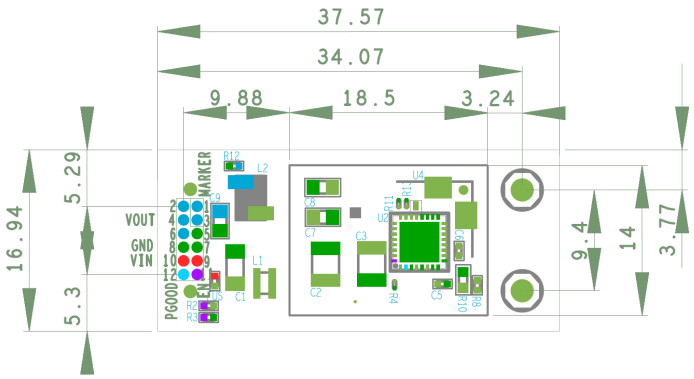
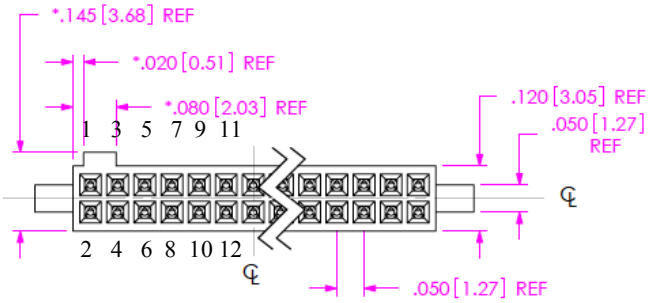


Figure 4: Top view of the FEASTMP module with mechanical dimensions.

Power connector

The FEASTMP module uses a 12-pin Samtec TFM-106-01-L-D-A male connector (the 'A' indicates the use of an alignment pin). The female mating connector is the SFM-106-01-L-D-A. All information about these connectors can be found in the Samtec web page (http://www.samtec.com/) under SFM or TFM, through hole, vertical, double row. In particular, at the time of releasing this document the footprint for the female connector could be found at http://www.samtec.com/documents/webfiles/cpdf/SFM-D-TH Footprint.pdf, while the outline of the connector at http://www.samtec.com/documents/webfiles/cpdf/SFM-1XX-XX-XXX-D-XXX-MKT.pdf. To avoid difficulties in procuring small quantities of the female connector, samples can be provided with the FEASTMP module on demand.

WARNING: users should refer exclusively to the pin numbering defined in this document, that is not the same defined by Samtec. In case of doubt, contact the DCDC support team.



Thermal interface

The bottom side of the module is equipped with a thermal interface of 10x10 mm in the form of exposed gnd plane. For the adequate operation of the module, this interface must be attached to a cooling element but electrically isolated from it. For this, an electrically insulating thermal pad must be inserted between the DCDC module and the receiving board (for instance the Bergquist Gap Pad 30S3000, Farnell code 878-3527). Pre-cut thermal pads of the appropriate size and thermal properties can be provided with the module as an optional on demand. It must be noted that, when the module connector male is mated to the female on the user's board, there is a separation of 5.97mm between the thermal interface and the surface of the user's board. In this space, the user must accommodate the cooling plate. A complete mechanical solution for that purpose has been developed and can be provided with the module as an optional. This solution is documented at the end of this document, under 'Optional parts'.

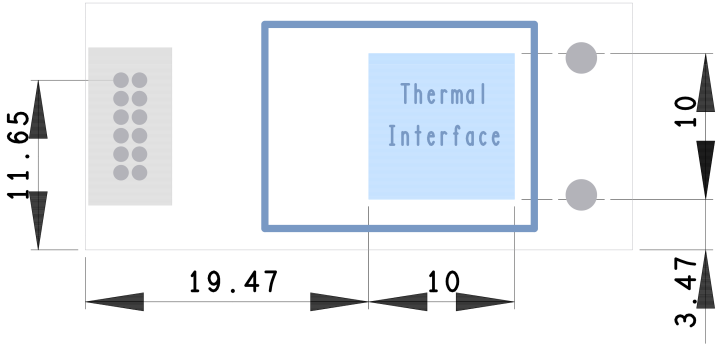


Figure 5: Top view of the module with size and position of the thermal interface.

Radiation tolerance

The radiation tolerance of FEASTMP is determined by the tolerance of the FEAST2 ASIC, which has been measured with different sources. Other than directly on FEAST2, these tests have been done on several generations of prototypes of the converter ASIC, obtaining very comparable results for TID and displacement damage.

Total Ionizing Dose

Samples have been exposed under bias at 25°C and -25°C, while biased at 10V input voltage and providing 2A current to a load. The radiation source was the CERN X-ray irradiation system accelerating 40keV electrons on a Tungsten target. The typical dose rate was 100krad(SiO_2)/min. An efficiency drop is the most evident effect, but it is limited to a 3-4% decrease in the worst case (without considering annealing, which improves the performance). Regulation performance is only slightly affected above 100Mrad(SiO_2). Thresholds of the UVLO, OCP, OTP systems are barely affected – shift of 100-200mV for UVLO, 0.3A for the OCP and 10°C for OTP after 500Mrad(SiO_2).

Displacement Damage

Displacement damage effects have been measured on previous prototypes during the development of the ASIC, as well as on 23 samples of the FEAST2 ASIC.

Two noticeable effects are induced by cumulative displacement damage, one affecting the on-chip linear regulator and the other the bandgap reference voltage generator.

Four liner regulators are integrated in FEASTs to generate the 3.3V required to power the on-chip control circuits. They all use p-channel MOS transistors as pass elements, and these transistors are strongly damaged by irradiation until the regulators fail. As a consequence, FEASTs stops correct functionality. This happens at an integrated flux above $5x10^{14}$ n/cm^2 (1MeV equivalent neutrons). The limit flux for failure is not known precisely. In tests at a nuclear reactor (Triga at JSI in Ljubljana) samples were working at 5 but not anymore at $6.5x10^{14}$ n/cm^2. In tests at the CERN PS irradiation facility (24 GeV/c protons) samples were still working at $8.5x10^{14}$ n/cm^2, one out of two was working at $1x10^{15}$ n/cm^2 and all samples exposed at larger integrated fluxes were failing. Uncertainty is added by the fact that the measured particle flux is translated into 1MeV neutron equivalent using a coefficient found in the literature (0.62 for the PS facility).

The bandgap voltage shifts with integrated particle flux, and this effect is traced to displacement damage since it was not observed at all during X-ray irradiation. This shift affects the output voltage regulated by the converter since this is referenced to the on-chip bandgap voltage.

Single Event Effects

SEE sensitivity has been measured with a Heavy Ion beam at CRC, Louvain-la-Neuve. Two samples were exposed at room temperature, with the available water cooling system to allow heat dissipation in the vacuum chamber, while providing 1 or 2 A to a load at 1.2 and 2.5 V. During the 5-hours irradiation, with Ar, Ni and Kr ions at different angles for effective Linear Energy Transfers (LETs) in the range of 10.2 to 65.2 MeVcm^{2}mg^{-1}, samples were exposed to a total integrated flux of about 126 million ions. FEAST2 constantly provided regulated power to the load all the time: no reset or functional interrupt was ever observed. However, small and short output disturbances (Single Event Transients, SET) were sometimes recorded. These were most often glitches below the nominal voltage; glitches above nominal were observed with smaller probability and amplitude, and were typically also shorter. Typical duration of the glitches was below 2us, and the amplitude never exceeded 20% of the nominal Vout. SETs exceeding 6% of the nominal voltage only occurred above a LET of 20 MeVcm^{2}mg^{-1}. In proton or neutron particle environments such as the LHC, SETs will hence be limited to amplitudes below 6%.

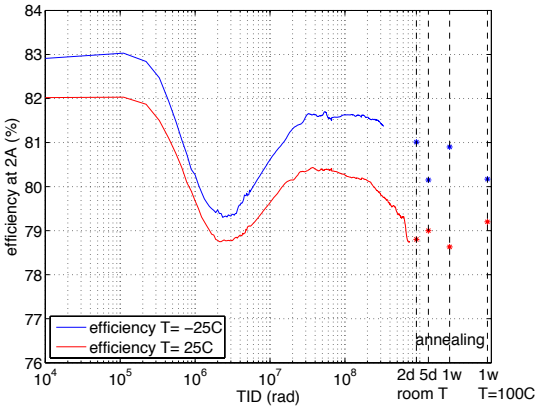


Figure 6: Efficiency variation with X-ray irradiation at the temperature of 25 and –25°C, for Vin=10V, Vout=2.5V and Iout=2A. Measurements are taken immediately after each irradiation step (no annealing). The last TID point for 25°C is at about 700Mrad(SiO_2).

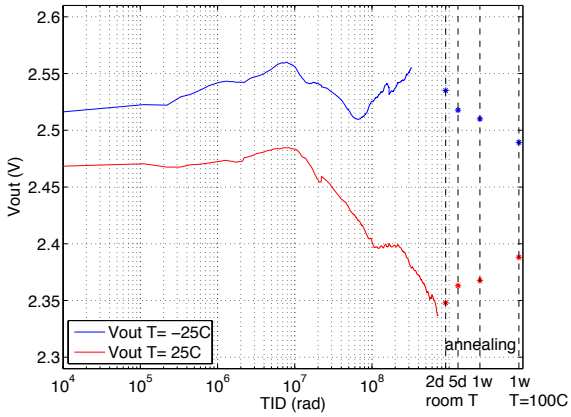


Figure 7: Output voltage variation with X-ray irradiation at 25 and –25°C, for Vin=10V, Vout=2.5V and Iout=2A. Measurements are taken immediately after each irradiation step (no annealing). The last TID point for 25°C is at about 700Mrad(SiO_2).

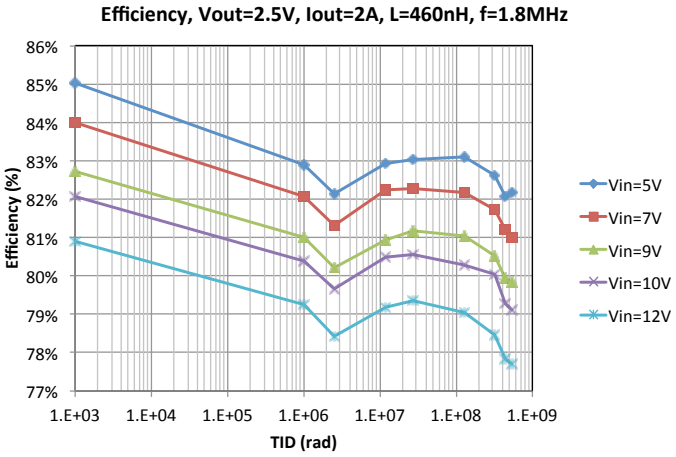


Figure 8: Efficiency variation with X-rays at 25°C, at different input voltages, and for 2A of load current (2.5V output). Last TID point is about 550Mrad(SiO_2). This module used the last ASIC prototype before the production-ready FEAST2.

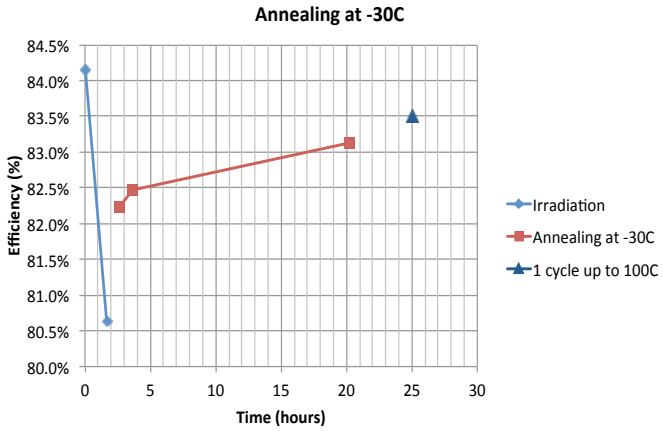


Figure 9: Annealing effect on the efficiency after an irradiation to 1.66Mrad(SiO_2) showing that the efficiency drop reported in the other figures and measured immediately after irradiation is an unrealistic worst case. In the real application, the efficiency drop is expected to be much smaller (if observable) due to annealing: efficiency already recovers in a few hours at cryogenic temperature. The cycle up to 100°C took about 15 minutes and contributed to a further recovery. This module used the last ASIC prototype before the production-ready FEAST2.

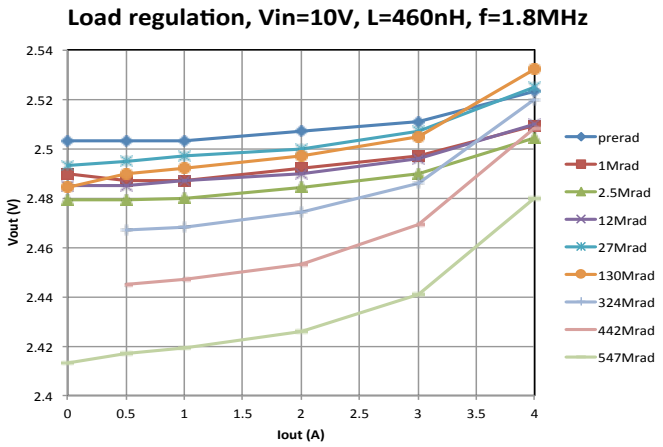


Figure 10: Load regulation variation with TID for an irradiation at 25°C. This refers to measurements taken on the module, before the output pi filter: the impact of the parasitic resistance of the filter's inductor and of the power connector is not included (but these do not change with TID). This module used the last ASIC prototype before the production-ready FEAST2.

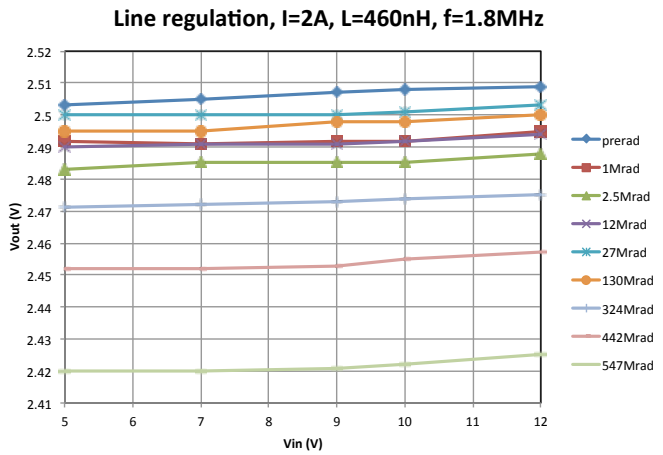


Figure 11: Line regulation variation with TID for an irradiation at 25°C. This module used the last ASIC prototype before the production-ready FEAST2.

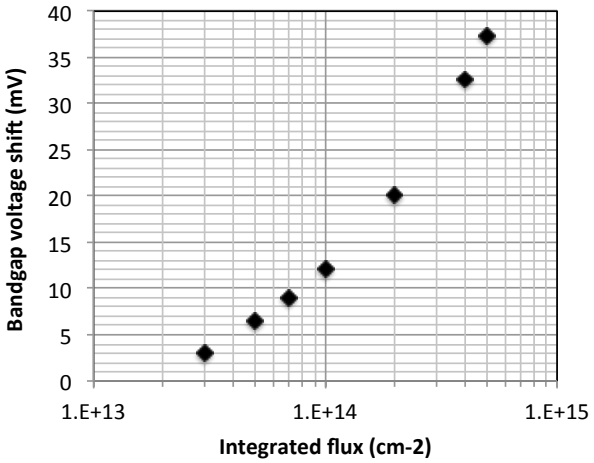


Figure 12: Variation of the bandgap voltage provided by the on-chip generator with integrated flux of particles (expressed as 1MeV equivalent neutrons). The reference voltage increases significantly, this effect being due to displacement damage, and as a consequence the output voltage regulated by the converter also increases. The pre-irradiation reference voltage is 0.6V. The last point is for an integrated flux of $5x10^{14}$ n/cm^2, samples irradiated beyond this level were not functional anymore because of the failure of the on-chip regulators providing the 3.3V supply to all the control circuits. This irradiation took place at the Triga reactor of JSI.

Typical operation waveforms

The figures in this section have been taken on a single module from a pre-production run using the FEAST prototype ASIC but they can be considered as typical also for the production modules with the FEAST2 ASIC. Comparison of several test points with the averages from the production testing of the first lot of 1000 FEASTMP modules has shown no relevant difference. The presented results are typical of a fresh (not irradiated) sample: for radiation-induced degradation please refer to the previous section (Radiation tolerance).

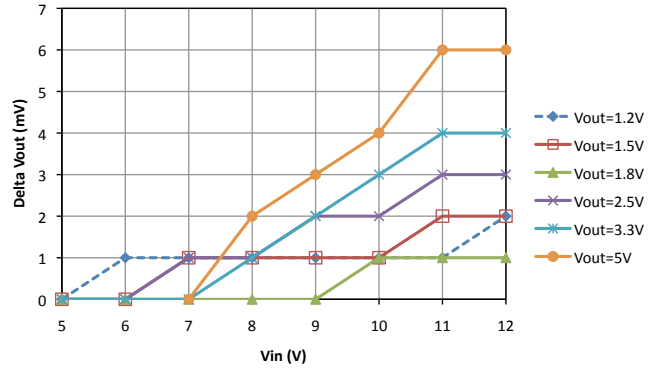


Figure 13: Line regulation for a load current of 2A with the module in good thermal contact with a cooling plate at about 18°C.

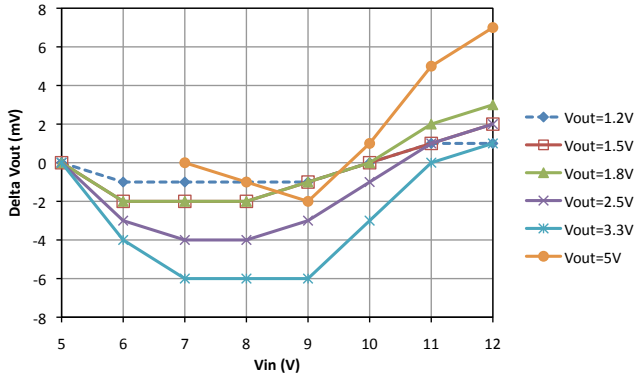


Figure 14: Line regulation for a load current of 4A with the module in good thermal contact with a cooling plate at about 18°C.

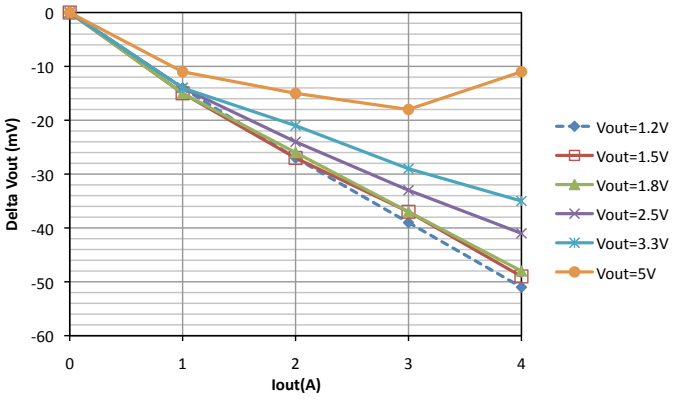


Figure 15: Load regulation for Vin=10V (very similar at all other input voltages). The drop is almost linear and it is due to the parasitic series resistance of the inductance of the output filter and of the power connector. At high output voltages, the linear decrease

is less pronounced because of the larger input current decreasing the voltage drop across the gnd pins of the power connector.

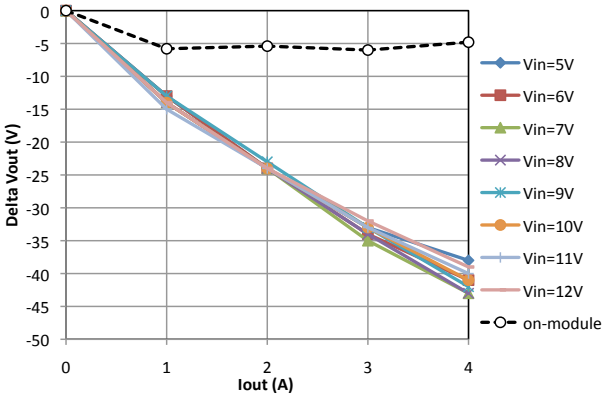


Figure 16: Load regulation for Vout=2.5V. The drop, independent on the input voltage, is almost linear and it is due to the parasitic series resistance of the inductance of the output filter and of the

power connector. The performance of the ASIC is shown in the dashed line, where Vout is measured on-module and before the output pi filter.

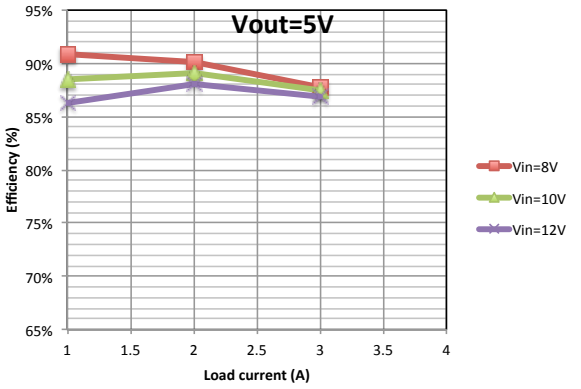


Figure 17: Efficiency for Vout=5V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C. The points at 3A are already beyond the max specified output power of 10W and are reported only for completeness. Vin needs to be at least 2V above Vout, therefore there is no curve for Vin=6V.

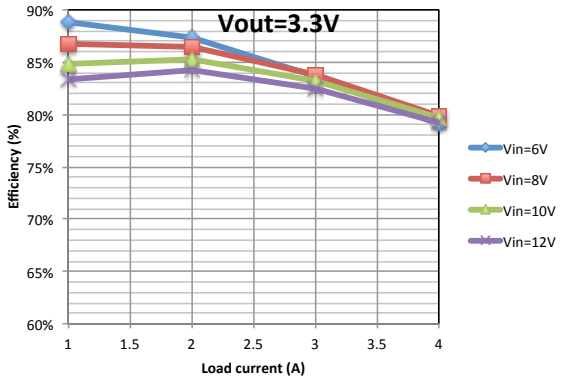


Figure 18: Efficiency for Vout=3.3V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C.

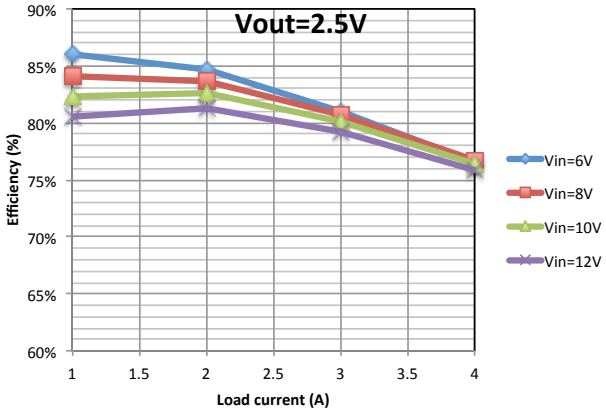


Figure 19: Efficiency for Vout=2.5V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C.

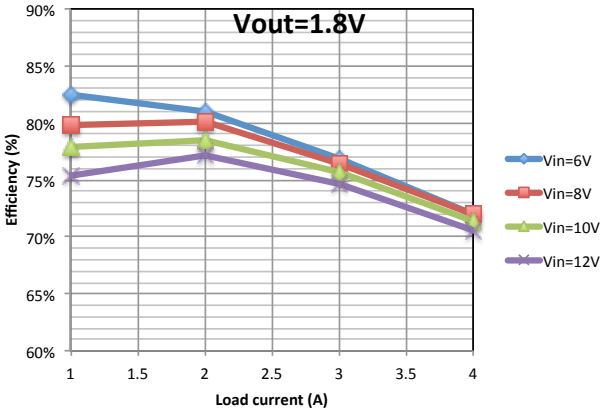


Figure 20: Efficiency for Vout=1.8V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C.

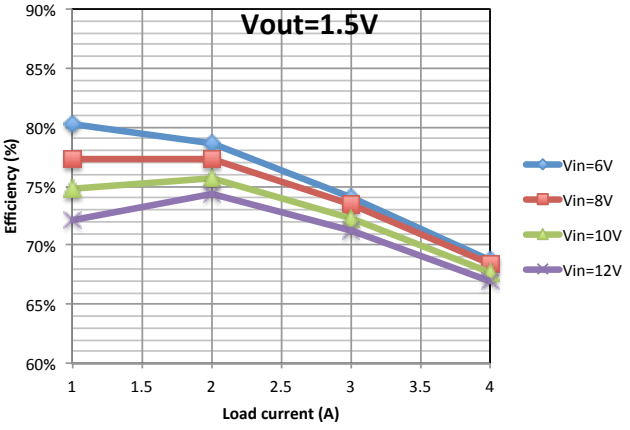


Figure 21: Efficiency for Vout=1.8V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C.

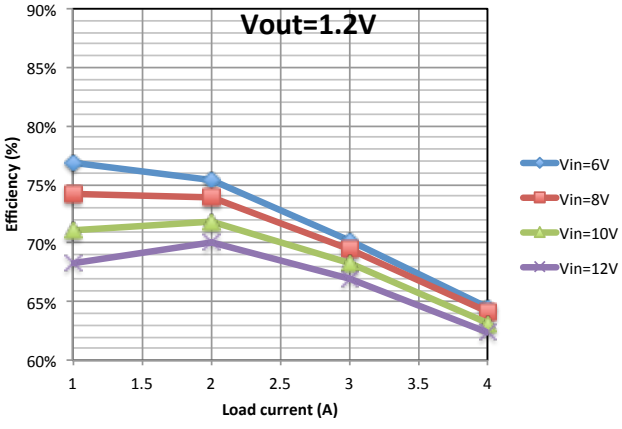


Figure 22: Efficiency for Vout=1.2V and different Vin and Iload with the module in good thermal contact with a cooling plate at about 18°C.

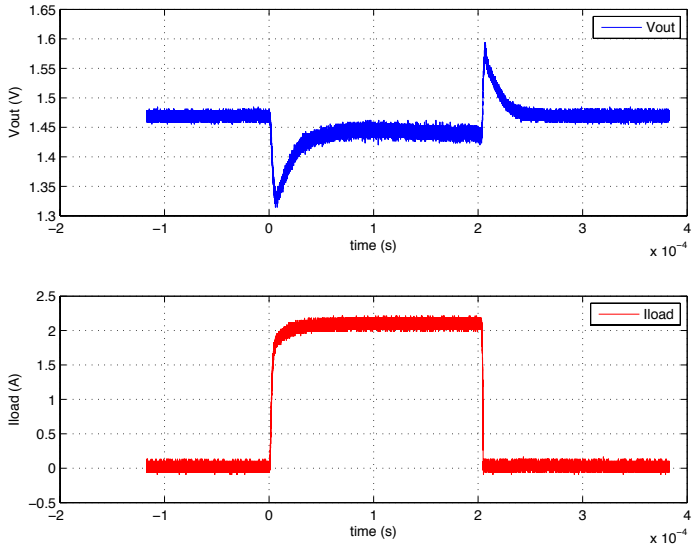


Figure 23: Transient load (0 to ~2A in ~5us) at Vout=1.5V. Vin=10V.

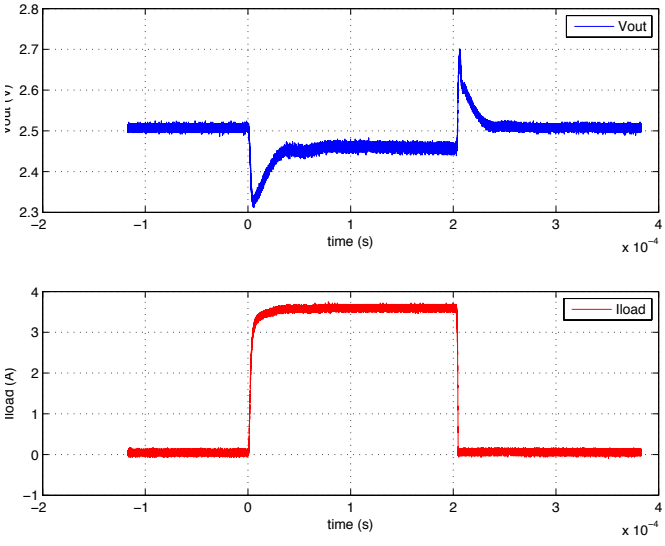


Figure 24: Transient load (0 to ~4A in ~5us) at Vout=2.5V. Vin=10V.

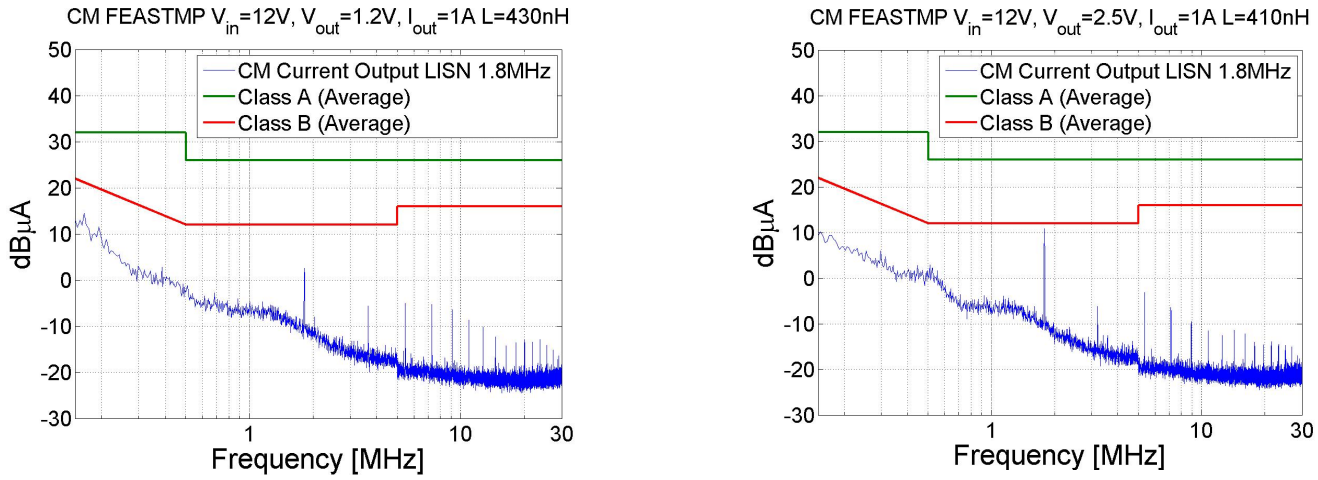


Figure 25: Output common mode current of the typical FEASTMP module at Vin=12V, Iout=1A, and for Vout of 1.2V (left) and 2.5V (right). Noise is kept below the Class B limit of the CISPR11 reference standard, with only the fundamental at the switching frequency exceeding 0 dBµA. Lowering the input voltage leads to a sensible decrease of the noise currents.

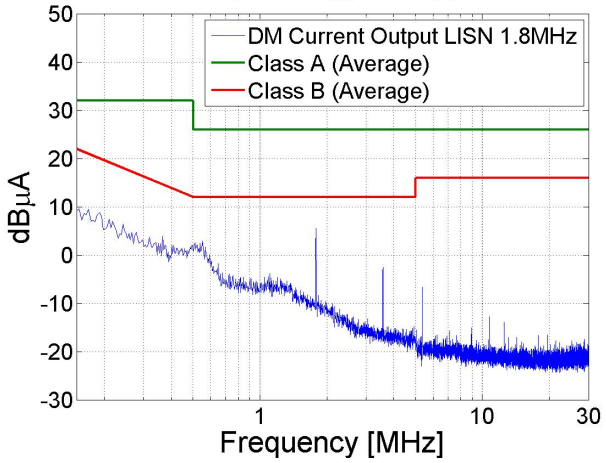


Figure 26: Output differential mode current of the typical FEASTMP module at Vin=12V, Iout =1A and for Vout=2.5V. All the noise properties shown are obtained with the shield mounted on the converter. In this configuration, the residual electric field radiated by the converter is not measurable with the equipment available.

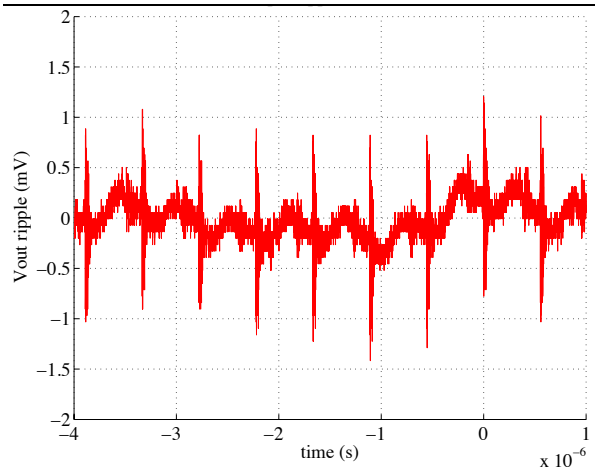


Figure 27: Output voltage ripple measured with an oscilloscope (AC coupled) with 20MHz bandwidth. Measurements conditions were Vin=10V, Vout=2.5V and Iout=2A.

Optional parts

This section lists the accessories that can be supplied on demand with each FEASTMP module to ease their procurement.

Mating female connector

The female mating connector from SAMTEC is the SFM-106-01-L-D-A. For small prototype quantities, and to facilitate procurement to the users, a limited number of connectors can be provided together with FEASTMP (one female mating connector per supplied module).

Thermal gap pad

To ensure good thermal contact with the cooling system (user-specific), a thermal interface material has to be added under the FEASTMP module. An exposed ground plane has been prepared for that purpose on the bottom side of the module, which should be in thermal contact with the cooling system but electrically isolated from it. During the whole development of the DCDC converter a thermal gap pad has been used for that purpose, evidencing very adequate thermal and mechanical properties. The material chosen is the Gap Pad 3000S30 from Bergquist, a soft gap filling material rated at a thermal conductivity of 3 W/m-K, at the thickness of 1mm. Once the final size and layout of the module was known, the adequate shape and size of the gap pad has been defined and a large number of pre-cut pads of this material has been procured. Pads can hence be supplied on demand together with any quantity of FEASTMP modules (prototype or even large-volume).

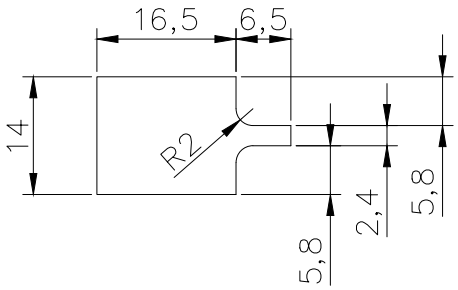


Figure 28: Shape of the pre-cut gap pad ensuring good thermal contact but electrical isolation between FEASTMP and the cooling system.

Figure 29: The pre-cut thermal pad, of a light blue color, is here positioned on top of a metal cooling plate fitting the FEASTMP module – the 2 screws fit the holes in the module and secure it to the metal plate that should be in contact with the cooling system.

Cooling interface plate

When the module connector male is mated to the female on the user's board, there is a separation of 5.97mm between the 10x10mm exposed ground pad under the FEASTMP module and the surface of the user's board. In this space, the user must accommodate a cooling plate and, to ensure good thermal contact, the pre-cut thermal gap pad. A complete mechanical solution for this purpose has been developed and can be provided with the module on demand. A 5mm thick Aluminum plate can be inserted in the 5.97mm separation and can be attached to the user's board with an Al screw (also supplied). This plate, mounted with the 1mm

thermal gap pad, perfectly fits the 5.97 mm gap space; however this plate must have an appropriate contact to the cooling system (user specific). The FEASTMP module can be secured to the metal plate with 2 screws, or with a spring clip custom-developed to match the plate that can also be supplied on demand. The following figures show the interface metal plate alone or with the FEASTMP module attached, and the technical drawings with all sizes.

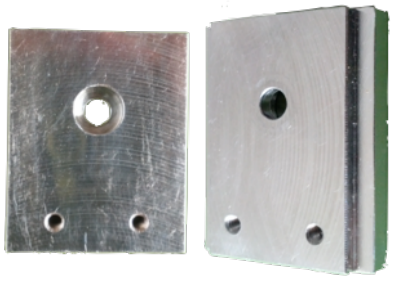


Figure 30: Top (left) and bottom (right) view of the cooling interface plate. The large single hole fits the supplied screw to attach the plate to the user's board and cooling system, while the pair of threaded holes can be used to fix the FEASTMP module to the plate (a pre-cut thermal gap pad has to be accommodated in between, as shown in Figure 29.

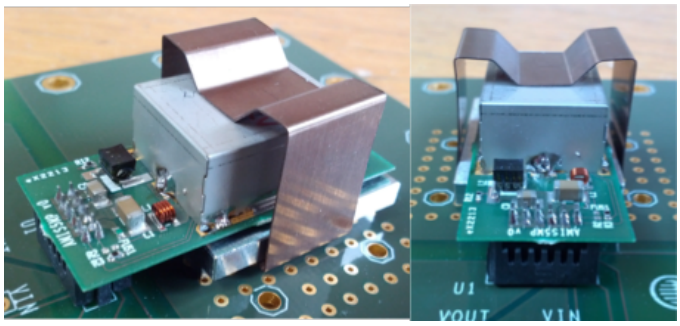


Figure 31: Views of the FEASTMP module connected to a sample user board and attached to the interface metal cooling plate with the help of the spring clip.

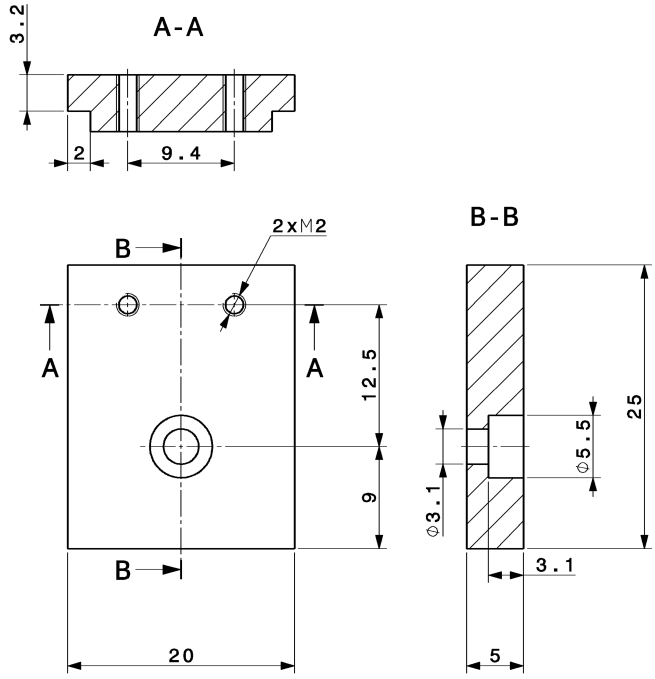


Figure 32: Technical drawing of the cooling interface plate.

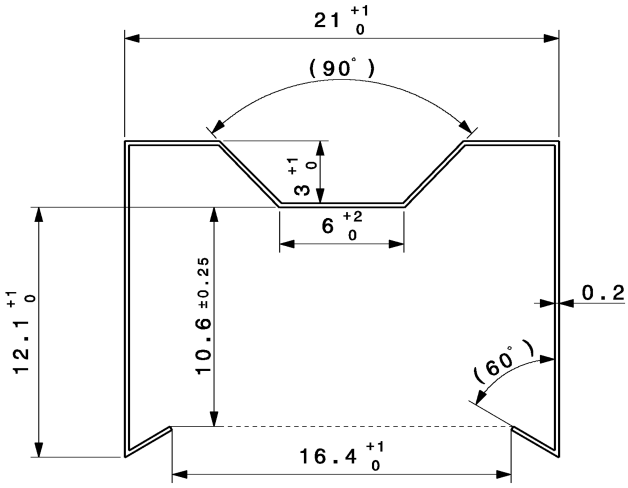


Figure 33: Technical drawing of the spring clip optionally attaching the FEASTMP module to the cooling interface plate. The clip is 12mm long.

Revision history

Revision	Date	Description
1.0	February2014	First release of the document.
2.0	July2014	Modifications to reflect the update of the FEASTMP module with the improved version of the ASIC, FEAST2. The tolerance to SEEs has been improved in FEAST2 and the PowerGood signal has been made compatible with 5V operation. This release of the datasheet also embeds results from the testing of the first production lot of 1000 modules. All distributed FEASTMP modules from July 2014 use FEAST2.
2.1	August 2016	Corrected the top view drawing of figure 4, and added the pin numbering warning for the main board connector. The FEAST2 ASIC has been modified to improve the production yield (there was a yield issue with the Power Good signal): The FEAST2.1 version has replaced the FEAST2 version in early 2016 for all new modules. This change is transparent to the users.