FEAST2.1

Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter

Features
- Input voltage range 5 to 12V
- Continuous 4A load capability
- Integrated Power N-channel MOSFETs
- Adjustable switching frequency 1-3MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Under-voltage lockup
- Over-Temperature protection
- Power Good output
- Enable Input
- Selectable Power Transistor size (5/5th or 2/5th) for improved efficiency at small loads (<600mA)
- Radiation tolerant: TID up to >200Mrad(Si), displacement damage up to $5{\cdot}10^{14}$n/cm^2 (1MeV-equivalent), continuous operation during exposure to heavy ions of LET up to 64MeVcm^{2}mg^{-1} with short transients below 20% of the nominal Vout (no destructive event, no output power interruption).

Applications

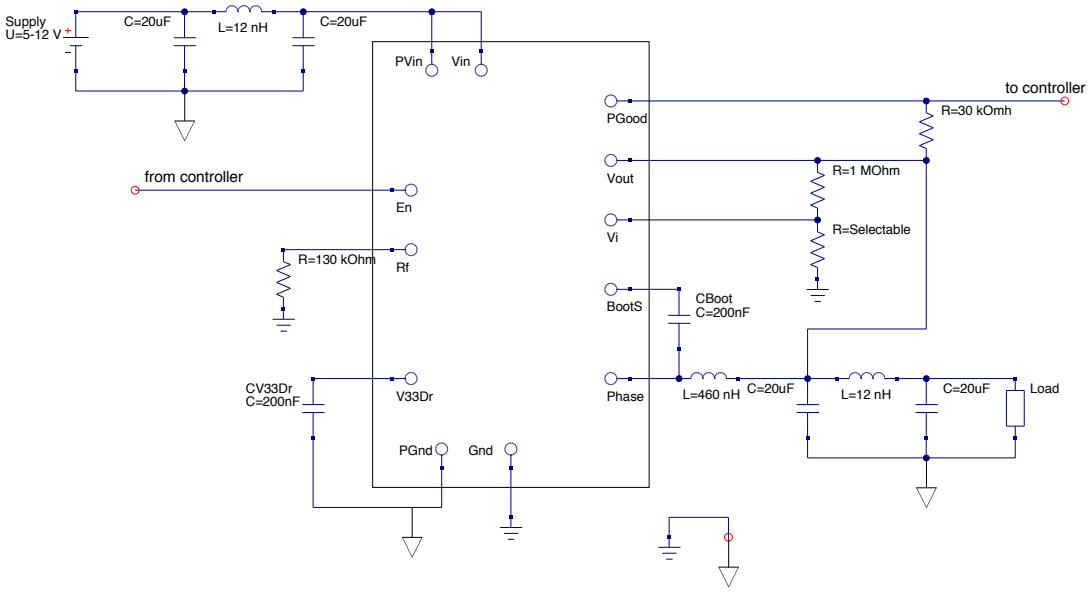
Point Of Load in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

Description

FEAST2.1 is a single-phase synchronous buck converter developed to provide an efficient solution for the distribution of power in High Energy Physics experiments. As such, it has been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the converter capable of continuous operation up to more than 200Mrad(Si) total ionizing dose and an integrated particle fluence of $5{\cdot}10^{14}$n/cm^2 (1MeV-equivalent). Single Event Effects resilience has been built-in, and the circuit has been tested free of destructive SEEs and of output power interruptions during irradiations with heavy ions up to an equivalent LET of 64MeVcm^{2}mg^{-1} (at 60^o incidence; no data available for higher LETs). FEAST2.1 has been designed for operation in a strong magnetic field in excess of 40,000 Gauss, and has been optimized for air-core inductors of 400-500nH: to be compatible with these small coil values, its switching operation is in the 1-3MHz range (1.5-2MHz for maximum efficiency).

The monolithic construction of FEAST2.1, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide POL regulation from a 5-12V supply rail. Its protection features include Over-Current, Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions. The chip temperature increase in the application can be monitored via a dedicated analog signal (PTAT).

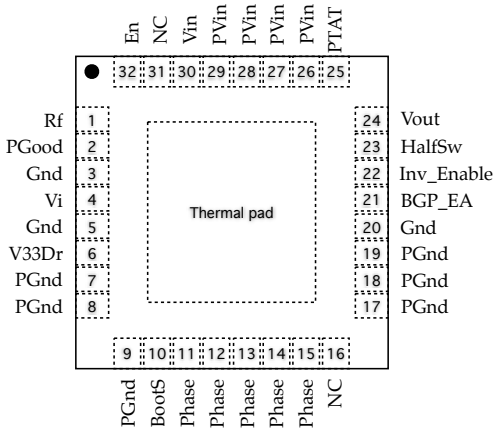
Typical application



Absolute Maximum Ratings

Power Input Voltage PVin……..…-0.3V to +12.0V
Control Input Voltage Vin……..…-0.3V to +12.0V
Bootstrap Voltage BootS……..…..-0.3 to PVin+3.6V
Phase Voltage…….0.3 V to Vin (DC), -2 to 13.5 V (AC, 10ns)
Phase to BootS Voltage……..…-0.3V to +3.6V
Driver Voltage, V33Dr..……..……..-0.3V to +3.6V
Feedback input Voltage of the E/A Vi…….……-0.3V to +3.6V
Frequency selector Rf……..….-0.3V to +3.6V
Power transistor size toggle HalfSw……..…….-0.3V to +3.6V
Reference voltage toggle Ref1V2……..…….-0.3V to +3.6V
Converter Enable En ……..……..…….-0.3V to +3.6V
Power good PGood……..……..……-0.3V to +6.0V
Output Voltage Vout……..……-0.3V to +6.0V
Current in PGood pin (when PGood is negated)…..……50uA

Pin Configuration



Top view - 32-lead plastic QFN (5x5 mm)
Thermal pad must be soldered to PCB PGnd

Pin Function

Rf (Pin 1): Frequency Selector. A resistor placed between this Pin and the board GND determines the switching frequency of the converter as illustrated in the following table. The recommended range for best performance is 1.5-2 MHz.

Resistance	Frequency
270K	1.03
200K	1.35
180K	1.48
160K	1.65
130K	1.99
100K	2.51
82K	2.98

PGood (Pin2): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 50uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window approximately ±6.5% around the selected Vout.

Gnd (Pin3, 5, 20): Ground of the control electronics of the converter. It must be connected to the PCB ground plane possibly in a location remote to the power current loop in the same plane.

Vi (Pin 4): Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 150kHz, but the DC regulation voltage Vout is selected by the addition of 2 resistors building a voltage divider between Vout and gnd. Vi is connected between the 2 resistors and the resulting voltage is compared to the internal reference voltage (about 0.6V). The resistor between Vout and Vi must have a value of 1MΩ, while the one between Vi and gnd is selectable (no resistor makes Vout = Vref).

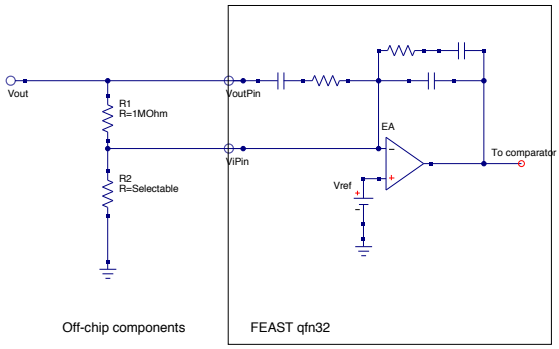


Figure 1: Configuring the output voltage.

V33Dr (Pin6): Voltage supply for the drivers of the power transistors. Although the regulator providing the 3.3V to the drivers is integrated, the large gate capacitance of the power switches requires a hefty charge storage element capable of providing quickly all the required transient current. This can not be achieved by on-chip capacitor, and an external capacitor of 220nF, positioned as close to the V33Dr pin as possible and directly connected to the PGnd (on the top PCB layer), is required.

PGnd (Pin 7, 8, 9, 17, 18, 19): Power Ground. This is the gnd of the power train and drivers, where large current transients are flowing. All PGnd pins must be connected to a large power plane under the qfn32, itself soldered to the Thermal Pad of the package, and connected to the PCB gnd plane by a large number of vias.

BootS (Pin 10): BootStrap capacitor voltage. FEAST2.1uses 2 NMOS transistors in the power train, and the High Side (HS) switch requires a BootStrap circuit, which is embedded, for correct gate driving (the gate has to be connected to Phase for turn-off and to Phase+3.3V for turn-on). Given the large size of the HS power switch, an off-chip capacitor is required to provide the transient current to the HS drivers during switching. This capacitor, of

220nF, must be positioned between Phase and BootS pins, as close as possible to the qfn32 package.

Bgp_EA (Pin 21): The reference voltage to the Error Amplifier is buffered and made observable at this pin exclusively for test purposes. It is recommended to leave this pin floating.

Inv_Enable (Pin 22): Toggle of the polarity of the Enable pin. If this pin is connected to gnd, the polarity of the Enable pin is switched. It is recommended to leave this pin floating.

HalfSW (Pin 23): Toggle controlling the size of the power train transistors. If this pin is connected to gnd, only $2/5^{th}$ of the integrated power switches are used, decreasing the power required to charge their large gate capacitance (increasing however their on-resistance). In this configuration, efficiency increases for light loads – below about 600mA. For larger loads, leave the pin floating for higher efficiency and reliability.

Vout (Pin 24): Regulated output voltage. This is an input pin bringing the Vout back to the converter's feedback circuit. It must be connected as specified in the description of Pin 4 (Vi).

PTAT (Pin 25): Proportional To Absolute Temperature provides and analog voltage whose variation with the chip junction T is linear with a slope of about 8.5 mV/^{o}C.

PVin (Pin 26, 27, 28, 29): Power Input Voltage. Input voltage of the power switches and drivers, where large current transients are flowing. Large input capacitances must be connected between this pin and PGnd as close to the package as possible (see board design recommendations later on).

Vin (Pin 31): Input Voltage for the control electronics of the converter. It is recommended to connect it to PVin close to the chip.

En (Pin 32): Enable input. FEAST2.1is normally disabled and requires a voltage above 850mV applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V. The polarity of the pin can be inverted by connecting Inv_Enable (Pin22) to gnd, in which case FEAST2.1is enabled for applied voltages below 850mV. Note that an embedded 500 kΩ resistor pulls the voltage of the En pin to gnd.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - PVin, Vin	5	11	V
Output voltage - Vout	0.9	5	V
Conversion ratio - Vout/Vin	2	10	
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	4	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	10	W
Switching frequency	1.5	2	MHz
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	^{o}C
Output current above which HalfSw should be left floating for higher efficiency and reliability	600	800	mA
Inductor value	400	500	nH
Enable voltage		3.3	V
Power Good voltage		3.3	V

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
PVin, Vin	Input voltage supply range	Converter operational	5	-	12	V
Iin	Input current for control electronics (via Vin pin)	En pin low, converter disabled	-	2	-	mA
Iout *(note1)*	Output current	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	1	A
		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18^{o}C	-	-	4	A
Pout *(note1)*	Output power	f=1.8MHz, L=460nH, package thermal pad soldered to PCB, PCB in air	-	-	2	W
		f=1.8MHz, L=460nH, good thermal contact with cooling plate at 18^{o}C	-	-	10	W

PWM						
DMax	Maximum Duty Cycle		-	100	-	%
DMin	Minimum Duty Cycle		-	0	-	%
Error Amplifier						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	20	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	10	-	V/µs
Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note2)*	-	4.79	-	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note2)*	-	4.52	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note2)*	-	815	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note2)*	-	730	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when FEAST2.1is not powered)		-	10	-	kΩ
Protections						
OCPpk	Over Current Protection peak level	Vin=10V, Vout=2.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18°C, *(note3)*	-	6	-	A
OCPavg	Over Current Protection average output current level	Vin=10V, Vout=2.5V, f=1.8MHz, L=460nH, Tcoolingpad≈18°C, *(note2, note4)*	-	4.8		A
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level, *(note5)*	-	103	-	°C
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level, *(note5)*	-	73	-	°C
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=10V, Vout=2.5V, f=1.8MHz, L=410nH, Tcoolingpad≈18°C, *(note2, note6)*		440		us
Power Good						
OV	Output Over Voltage PGood upper threshold			+6.5		%
UV	Output Under Voltage PGood lower threshold			-6.5		%
Proportional To Absolute Temperature signal						
PTAT	Analog output voltage	Converter disabled, environmental T sweep		8.5		mV/°C

Notes

Note 1: Max rated output current only allowed if max output power is not exceeded.
Note 2: Average value taken from measurements on 10 samples from the production run.
Note 3: This value has not been measured precisely and is reported as approximate indication of the peak current detection for OCP. The peak value does not have relevant dependence on Vin and Vout.
Note 4: The OCP uses a peak detector, hence the average output current for OCP detection depends on the input and output voltages. In particular, the OCP detection current for Vin=10V is not significantly different for Vout of 2.5-5V, whilst it increases by about 10% at 1.8V and even further at smaller output voltages.
Note 5: The threshold temperature for OTP is approximate, since it is not measured on-chip (no junction T available when the measurements have been done, on version 2.0 of FEAST). Fully assembled FEASTMP boards regulating 2.5V with no load were put in good thermal contact with a thermal chuck, and T was increased. The temperature of the chuck when the FEASTMP module turned off (and back on) was taken as threshold.
Note 6: The duration of the Soft Start does not have a relevant dependence on Vin and Vout.

Block Diagram

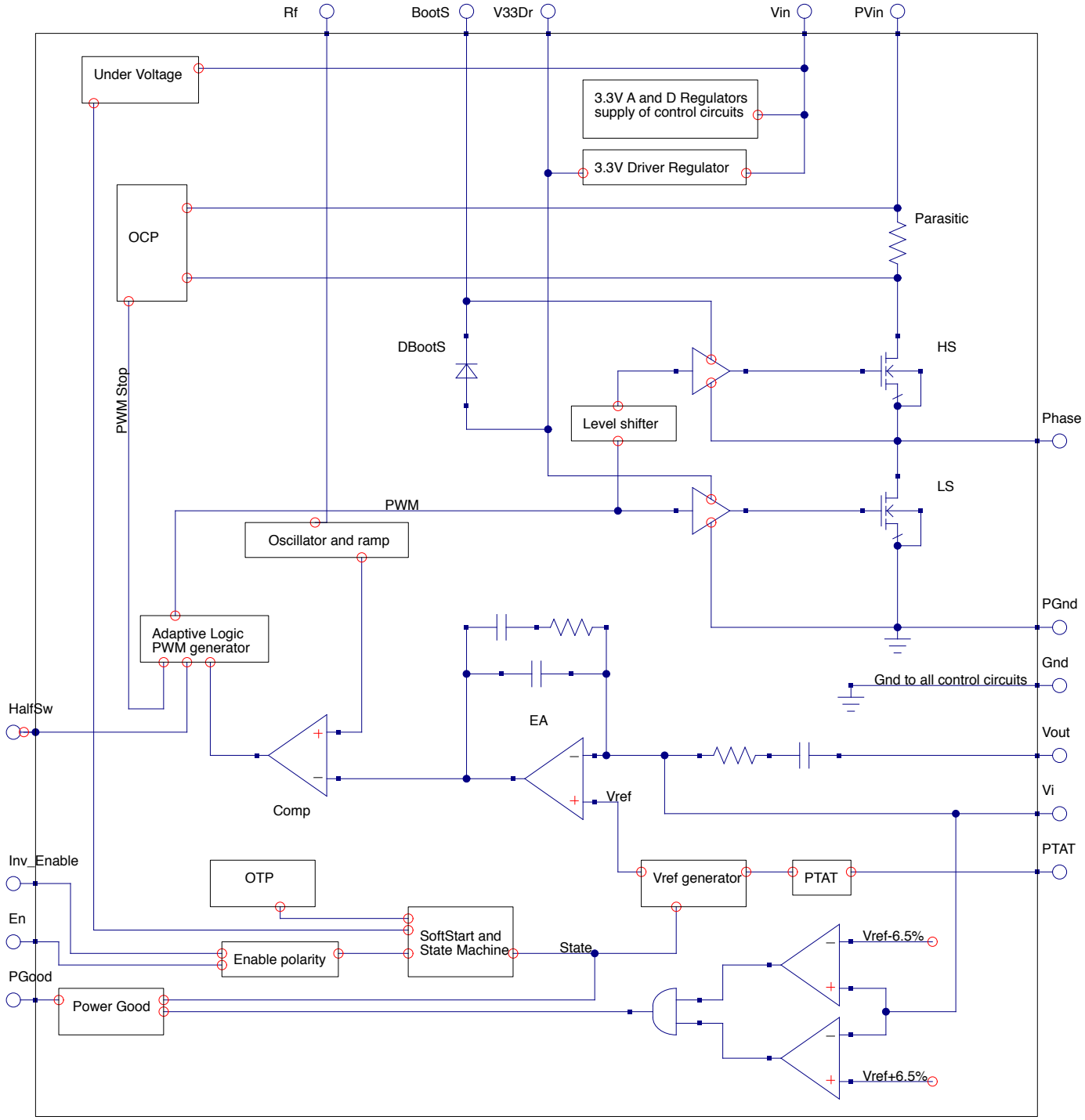


Figure 2: Block diagram of the FEAST2.1ASIC.

Operation

FEAST2.1is a DCDC converter designed specifically for application in the high radiation and magnetic field of experiments in High Energy Physics. Radiation tolerance is a particularly difficult target for a DCDC converter, and its achievement required to compromise on other performances typically important in similar components in the commercial marketplace. The typical application at steady large load current with power provided from a remote supply (not from a battery) implies very relaxed requirements on quiescent current, while a fast feedback loop is at premium for some detectors where current consumption might have an instantaneous threefold increase.
Designed to be embedded in a custom DCDC module and distributed in this form to users, FEAST2.1has not been designed and tested for allowing large freedom in the choice of the external components (capacitors, inductors and resistors). Moreover, its use in an environment very sensitive to conducted and radiated noise in a physics experiments demands large expertise in EMC design since the position and choice of all components has large influence on the final detector performance. It is hence strongly advised not to procure FEAST2.1in its stand-alone packaged form but to use the available full DCDC converter module which has been qualified for class-B conducted noise (CISPR11) and has been shown to be well compatible with integration in very close proximity to the sensitive readout electronics of even the tracker silicon detectors. The module exists in both positive (FEASTMP) and negative (FEASTMN) output voltage versions, and datasheets can be found under the public web page of the DCDC PH-ESE project: http://project-dcdc.web.cern.ch.

Output voltage selection
The output voltage is determined by the choice of the 2 resistors in voltage divider configuration between Vout and gnd (Figure 1). In doing so, it is important to know as precisely as possible the value of the reference voltage to the Error Amplifier. This has been measured on 40 tests points on each production wafer. The average value over the 6 wafers is 599mV with a standard deviation of 5.7mV (minimum measured: 583mV; maximum measured: 613mV).

Switching frequency
The switching frequency of the converter can be adjusted with one external resistor, which provides the bias current to the embedded oscillator. Although FEAST2.1has been tested as functional over a wide range of frequency (1 to 3.5MHz), best performance is achieved in the range of 1.5-2MHz. At lower frequency, the peak-peak current in the small air-core inductor increases excessively and determines useless losses and possibly an early onset of the OCP. At higher frequency, driving losses increases dramatically and make the efficiency drop very sensibly. While usage at 1.5MHz allows top efficiency, 1.8MHz operation allows for reduced conductive noise and is preferred as default configuration.

Embedded linear regulators
While it can operate from a supply voltage of up to 12V, the control electronics in FEAST2.1requires powering at 3.3V. A number of linear regulators are embedded to provide appropriate voltage to the drivers of the power transistors, to the bandgap and reference current generator, to the analog and to the digital circuitry. With the exception of the voltage regulation for the power transistors' drivers, all storage capacitors required for the regulators are on-chip and have been sized to ensure steady voltage even during large current surges.

Under-Voltage lockout
The embedded linear regulators need a sufficient level of over-voltage to provide stable 3.3V voltage to the control circuitry. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above about 4.8V (on rising Vin). This comparator has an hysteresis and FEAST2.1is disabled again when, for falling Vin, the input voltage drops below about 4.5V.

Enabling FEAST2
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has not been asserted by applying a voltage above about 820mV. FEAST2.1can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each FEAST2.1providing regulated power to a different load). The polarity of the enable signal can however be inverted by connecting the Inv_Enable pin to gnd. In this case, the circuit is disabled when a voltage above 820mV is applied to the enable (En) pin; it is hence enabled by default if the En pin is floating – an internal pull-down resistor of 500 kΩ keeps the voltage of the pin to gnd.

Soft Start procedure
When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the reference voltage of the EA, the output voltage reaching the nominal value in about 440us in the nominal configuration using the 0.6V bandgap (at the switching frequency of 1.8MHz, this time varying inverse linearly with frequency). Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that FEAST2.1is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 3.3V, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, in reset and when the output voltage is outside a ±6.5% window around nominal. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 50uA, so an appropriate pull-up network has to be selected. The absolute maximum voltage on the PG pin is 3.6V.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip junction temperature and disables FEAST2.1when it reaches about 103°C (the OTP temperatures are not precisely measured since T is not measured on FEAST2.1itself). The OTP has a hysteresis of about 30°C, hence the converter restarts (with SS) when the junction temperature decreases below 73°C. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

Over-Current Protection (OCP)
OCP is integrated as a real peak detector on the current flowing during each cycle in the HS transistor. Current sensing takes place on the parasitic resistance of metal lines bringing the input current from the input pads to the HS transistor. When the instantaneous current exceeds about 6A (very approximate value), the PWM is reset and forces the HS to turn off. If the excessive load current condition persists, the on-time of the HS is not determined anymore by the feedback loop (which would require longer on-times to provide more output power) but by the OCP, and as a consequence the output voltage drops. This condition might endure as a steady state, PG being pulled to gnd if the output voltage drop exceeds 6.5% of the nominal. The peak current of 6A translates in different average output current depending on the input and output voltage, frequency and inductor value.

Compensation network
The compensation network is fully integrated and determines a typical loop bandwidth of about 150kHz in the recommended operation environment (frequency, voltages, inductor, on-board passives). FEAST2.1is hence capable of quickly adjusting the output voltage in case of output load transients.

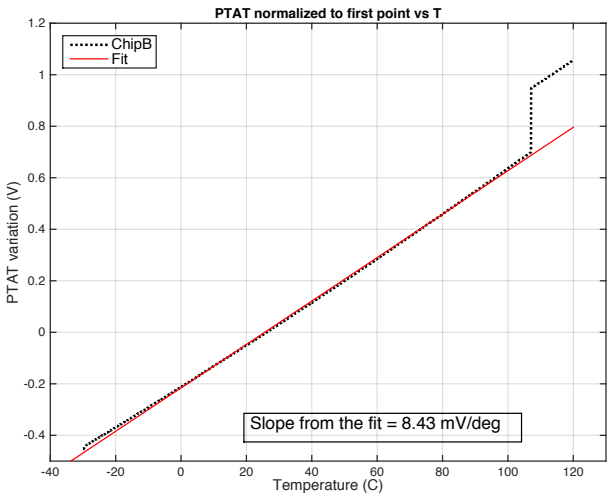
Cooling
FEAST2.1is specified for operation up to 10W output power. With an efficiency of 80% in case of large load current and not–cryogenic cooling, this translates in more than 2W lost in the converter (including the resistance of the inductor and of other passive components). Most of this power is burnt by FEAST2.1itself and needs to be transferred to the cooling system efficiently. The chosen qfn32 package has an exposed cooling pad to which the IC is directly attached, and the pad must be soldered to the gnd plane of the PCB which itself must have a good thermal contact to the cooling system.

Operation at small output current
The size of the power transistors has been chosen for optimum efficiency in the output current range of 1.5-2.5A. For small output currents the excessive size of the transistors induces a large penalty in efficiency, since their large gate capacitance has to be charged at every switching cycle (large driving losses). To partially reduce the losses associated to the large size of the power train, it is possible to stop a fraction of the drivers by pulling down (to gnd) the HalfSw pin. In this way, only 2/5th of the HS and LS transistors are switching, increasing their effective on-resistance (not too relevant for small load currents) but saving switching power. This is power efficient at small loads, up to about 800mA, as shown in the table below referring to Vin=10V, Vout=2.5V, f=1.8MHz, L=460nH.

	Efficiency (%)	
Iout (mA)	HalfSw floating	HalfSw grounded
100	39.3%	44.6%
200	56.5%	61.0%
300	64.6%	68.1%
400	69.9%	73.0%
500	73.7%	75.8%
600	76.8%	77.7%
700	78.5%	79.4%
800	79.6%	80.1%
900	80.2%	80.4%
1000	80.8%	80.4%

Proportional To Absolute Temperature (PTAT) voltage

The PTAT analog signal can be used to monitor the T increase of the FEAST2.1 ASIC during operation, in particular to verify that the cooling is appropriate. The absolute value of the PTAT voltage at a given T has a wide sample-to-sample variability. However, the PTAT increase with respect to T is very close to a straight line with slope 8.5 mV/°C. This has been verified on 4 samples from 2 different manufacturing lots: although the PTAT value at the same T could vary by 200mV, all samples had a linear dependence between **Δ**PTAT and **Δ**T, with a very similar slope (averaging 8.5). This linear relation is shown for one of the measured samples in the figure below. The discontinuity above 100°C happens when the OTP sets in and is due to an hysteresis inserted because of the over-T protection. The vertical scale has an origin at about 25°C in this case because the PTAT variation has been arbitrarily referred to the value at that T. Given the variability in the absolute value of the PTAT, it is possible that some sample outputs a 0V signal for very low T and only start to the linear relation at higher temperature. In our tests, this happened in one sample (0V output between -30 and -18°C).



Radiation tolerance
The full development of FEAST2.1has been driven by the radiation tolerance goal of reliable flawless operation in the HEP experiments at the CERN Large Hadron Collider (LHC). In particular, radiation tolerance specifications for applications in phase1 upgrades of the LHC include TID up to 20Mrad, displacement damage up to 2.5e14 particles/cm^2 (1MeV n-equivalent), no destructive event (SEB, SEGR) and continuous supply of the correct output voltage in a hadron radiation environment (no SETs on the output beyond ±20% of the nominal regulated voltage).
Radiation tolerance determined in the first place the choice of the CMOS technology used for the design: high-voltage transistors were required not to be sensitive to SEB and SEGR during heavy ion tests up to an LET of 30MeVmg^{-1}cm^2 (at normal incidence).

For the control circuits, Hardness By Design (HBD) techniques have been systematically used to prevent the opening of leakage currents with TID. Results of SEE test campaigns at heavy ion and pulsed laser facilities enabled the measurement of the cross-section and the localization of weak points during the development, and were used to correct the final design.
Full radiation characterization has been done on FEAST2.1prototypes mounted on full DCDC modules of the FEASTMP type. The results of the characterization are reported in the datasheet of the FEASTMP module that can be found in the public web page of the DCDC converter project: http://project-dcdc.web.cern.ch. Please refer to that document for full radiation tolerance results.

Typical operation waveforms

Full characterization of the FEAST2.1ASIC has been done on prototypes mounted on full DCDC modules of the FEASTMP type. The results of the characterization are reported in the datasheet of the FEASTMP module that can be found in the public web page of the DCDC converter project: http://project-dcdc.web.cern.ch. Please refer to that document to find all waveforms for typical operation of the converter.

Package description

FEAST2.1is packaged in a plastic Quad Flat No-Lead (QFN) package 5.0x5.0x0.9mm in size, with 32 pads and with an exposed pad to be soldered to the PCB for better thermal properties. The package is rated for a chip temperature increase of 27 to 31 ^{o}C/W depending on the air flow. The suggested PCB layout for the integration of FEAST2.1is shown in the following figure. The dimension of the signal pads is 0.25x0.5mm and the one of the central exposed thermal pad is 3.6x3.6mm. All distances are referred to the center of the signal or exposed thermal pads.

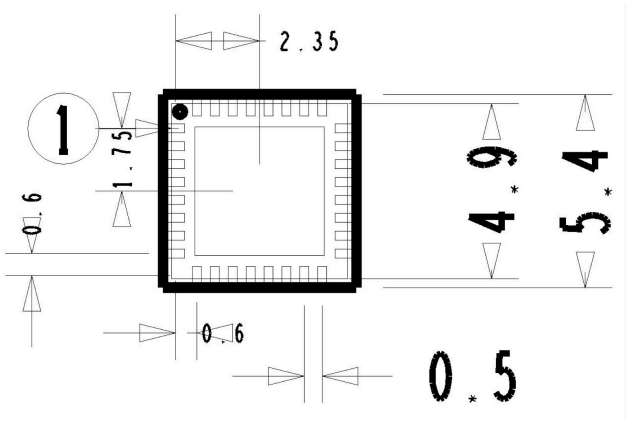


Figure 3: Suggested PCB layout for the integration of the FEAST2.1QFN32 package.

Revision history

Revision	Date	Description
1.0	June 2016	First release of the document.