AMIS5MP

Radiation and magnetic field tolerant 12V 4A DC/DC converter module

Features
- Input voltage range 6 to 12V
- Continuous 4A load capability (dependent on output power level, limited to 10W)
- Available in different output voltage versions from 1.2 to 3.3V
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Input under-voltage lockup
- Over-Temperature protection
- Power Good output
- Enable Input
- EMC: conducted noise compatible with Class-B CISPR11 requirements
- Shielded to make it compatible with operation in close proximity (1cm) to sensitive detector systems
- Radiation tolerant: TID up to >200Mrad(Si), displacement damage up to 7e14n/cm^2 (1MeV-equivalent), no destructive SEEs up to >30MeVcm^{2}mg^{-1}
- Magnetic field tolerance in excess of 40,000 Gauss

Applications
- Point Of Load)POL) converter for prototype electronics systems of HEP detector upgrades (the module is not production ready and must not be relied upon for applications in systems contributing to physics data taking).

Description

AMIS5MP is a full DC/DC converter module built around the AMIS5 DC/DC radiation-tolerant ASIC to the purpose of providing HEP experiments with representative prototype converter modules for system tests in view of detector upgrades. AMIS5 is not yet the final ASIC approved for mass production, but an advanced prototype available since August 2012. It has been tested fully and several modifications were implemented either to correct undesired features, or to add more advanced functions. While waiting for fabrication and qualification of the new ASIC, it was deemed important to provide interested users with a representative DC/DC converter module pin-to-pin compatible with the mass-production one that will possibly be available in early 2014.

Although AMIS5MP does not use the production-ready ASIC, its full construction is extremely close to the one planned for the final modules. The PCB design and choice of the passives, determining the EMC properties of the module, will not be changed significantly. The custom air-core inductor, a 460nH oval toroid manufactured by Coilcraft, is the final design. The 125um thick Cu shield is also production-ready, as well as the Samtec 12-pin connector.

At the heart of the AMIS5MP module, the AMIS5 ASIC been designed for flawless functionality in a harsh radiation and magnetic field environment. The selection of an appropriate CMOS technology, coupled to the systematic use of Radiation Hardness By Design (RHBD) techniques, makes the converter capable of continuous operation up to more than 200Mrad(Si) total ionizing dose and an integrated particle fluence of 7e14n/cm^2 (1MeV-equivalent). Single Event Effects resilience has been tested at a Heavy Ion irradiation facility, showing that the circuit is free of destructive SEEs up to an LET of 30MeVcm^{2}mg^{-1} at normal incidence (no data available for higher LETs). However, a large sensitivity to Functional Interrupt (SEFI) has been detected at even low LETs, indicating a possibly large rate of failures in some applications. The origin of this sensitivity has been investigated with pulsed laser tests, and has been removed in the new ASIC design.

AMIS5MP has been designed for operation in a strong magnetic field in excess of 40,000 Gauss: its coils (the main energy storage element of 460nH and 2 inductors in the input-output filters) are air-core. Given the small inductance of the main coil, the switching frequency is set at about 1.8MHz.

The monolithic construction of AMIS5, with the integration of the power train and the bootstrap diode with the controller, makes the converter a space-efficient solution to provide POL regulation from a 6-12V supply rail. Its protection features include Over-Current, Over-Temperature and Under-Voltage to improve system-level security in the event of fault conditions.

Note on this datasheet

AMIS5MP is a prototype intended for distribution and use for a very limited time (a few months), since it will be replaced in early 2014 by production-ready modules with the new ASIC. For this reason, there has been no effort in measuring the performance of a large number of samples and average the results to be specified on this datasheet. Quoted performance refers hence to measurements obtained on a few modules, which explains why there is no indication on min and max values for most electrical specifications.

Absolute Maximum Ratings

Power Input Voltage, PVin……..…….-0.3V to +12.0V
Converter Enable, En ……..……..-0.3V to +3.6V
Power good, PGood……..……-0.3V to +3.6V
Output Voltage, Vout…….-0.3V to +3.6V

Pin Configuration

Pin Number	Function
12	PGood
11	En
1,2,3,4,6	Vout
5,7,8	Gnd
9,10	Vin

Pin Function

PGood (Pin12): Power Good flag. This output pin comes from an open-drain NMOS transistor that is conductive when the converter is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider if the CMOS logic level required for the PGood signal is below Vout. The value of the pull-up resistor determines the current in the open-drain NMOS, which should be limited below 50uA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disable mode, during Soft Start (SS), in case of under-voltage, over-temperature, or over-current. In case the pull-up resistor is not connected to Vout but to another available voltage supply, it is possible that the PG signal is asserted when the converter is not properly powered (in this case, there is no valid voltage on-chip to bias the gate of the open-drain NMOS, which can hence not drive the PG signal to gnd).

En (Pin11): Enable input. AMIS5MP in normally disabled and requires a voltage above 800mV applied to this pin to be enabled and start operation. This voltage value has been chosen to make the pin compatible with control from almost any CMOS logic controller between 0.9 and 3.3V.

Gnd (Pin 5, 7, 8): Ground of the converter.

Vout (Pin 1, 2, 3, 4, 6): Regulated output voltage.

Vin (Pin 9, 10): Power Input Voltage.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - PVin, Vin	6	11	V
Output voltage - Vout	1.2	3.3	V
Conversion ratio - Vout/Vin	2	10	
Output current – Iout (supposes efficient cooling of PCB ground plane)	0	4	A
Output power – Pout (supposes efficient cooling of PCB ground plane)	0	10	W
Cooling plate temperature (temperature of the PCB ground plane that has to be attached to a cooling plate)	-40	30	^{o}C

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
PVin, Vin	Input voltage supply range	Converter operational	6	-	12	V
Iout *(note1)*	Output current	Vin=10V, Vout=2.5V, PCB in air	-	-	1	A
		Vin=10V, Vout=2.5V, good thermal contact with cooling plate at 18^{o}C	-	-	4	A
Pout *(note1)*	Output power	Vin=10V, Vout=2.5V, PCB in air	-	-	2	W
		Vin=10V, Vout=2.5V, good thermal contact with cooling plate at 18^{o}C	-	-	10	W
Input Under-Voltage Lockout						
VinStartTh	Vin start threshold	Vin rising trip level *(note2)*	-	5	-	V
VinStopTh	Vin stop threshold	Vin falling trip level *(note2)*	-	4	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level *(note2)*	-	780	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level *(note2)*	-	720	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when FEAST is not powered)		-	10	-	kΩ
Protections						

OCPpk	Over Current Protection peak level	Vin=10V, Vout=2.5V, Tj=25°C, *(note2)*	-	8.5	-	A
OCPavg	Over Current Protection average output current level	Vin=10V, Vout=2.5V, Tj=25°C, *(note2)*	-	6.5		A
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level, *(note2)*	-	115	-	°C
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level, *(note2)*	-	85	-	°C
Soft Start						
SSt	Duration of the Soft Start procedure to reach regulation at nominal Vout	Vin=10V, Vout=2.5V, Tj=25°C	-	1	-	ms

Notes
Note 1: Max rated output current only allowed if max output power is not exceeded
Note 2: Measured on xx boards from the production run

Operation

Switching frequency
The switching frequency of the converter is adjusted on-board with one resistor, which provides the bias current to the on-chip oscillator. No intervention is required to the user and the nominal frequency is set to 1.8MHz.

Input Under-Voltage lockout
The on-chip linear regulators providing the appropriate 3.3V to the control electronics need a sufficient level of over-voltage for proper operation. To prevent faulty operation because of lack of appropriate supply to the control electronics, an on-chip comparator only enables operation of the circuit when the input voltage is above 5V (on rising Vin). This comparator has a large hysteresis and AMIS5MP is disabled again when, for falling Vin, the input voltage drops below 4V.

Enabling AMIS5MP
The circuit is disabled by default, so it will not start when a sufficient Vin is applied to its input unless the available enable pin (En) has been asserted by applying a voltage above 800mV. AMIS5MP can hence be turned on-off by a control signal without the need for removing the power to its Vin bus, which makes easy its parallelization on the same supply bus (each AMIS5MP providing regulated power to a different load).

Soft Start procedure
When the converter is enabled a large current is required to charge the output capacitors to the nominal regulated voltage. This current has to be limited to avoid circuit damage. A pre-defined Soft Start (SS) procedure takes care of limiting the inrush current by gently increasing the on-chip reference voltage of the EA, the output voltage reaching the nominal value in about 1ms. Every time the converter is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows a hard-wired sequence to reach the state where it efficiently regulates the output voltage. This sequence is controlled by an embedded 2-bits state machine. SS takes place in the third of the 4 states and finishes when the rising reference voltage slightly exceeds the bandgap reference voltage. At this time, the reference to the EA is switched to the steady reference generator (bandgap). It is hence normal to observe a small decreasing voltage step in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that AMIS5 is not in a faulty state. For easy compatibility with almost any CMOS logic level, this output is an open drain (of an NMOS transistor). This transistor is normally disabled when the converter is regulating correctly, while it is turned on otherwise: in disabled state (En pin low), in OTP, in OCP. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG to rise in this condition it is recommended to use Vout as pull-up voltage (either directly or via a voltage divider). Current in the NMOS pull-down transistor has to be limited below 50uA, so an appropriate pull-up network has to be selected.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the on-chip junction temperature and disables AMIS5 when it reaches 120°C. The OTP has a hysteresis of about 35°C, hence the converter restarts (with SS) when the junction temperature decreases below 85°C. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

Over-Current Protection (OCP)
OCP is integrated as a real peak detector on the current flowing during each cycle from Vin: when the instantaneous current exceeds about 8.5A, the OCP sets in. As a consequence, Vout drops below nominal regulation value. This condition might endure as a steady state, PG being pulled to gnd. The peak current of 8.5A translates in different average output current depending on the input and output voltage, but it is typically around 6A.

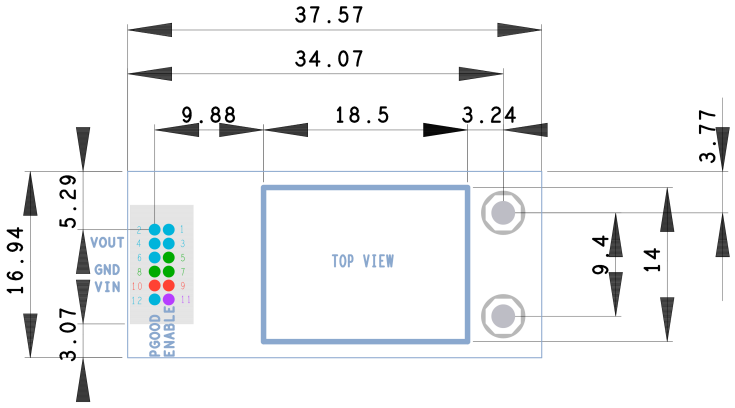
Compensation network
The compensation network is fully integrated on-chip and determines a typical loop bandwidth of about 150kHz. AMIS5MP is hence capable of quickly adjusting the output voltage in case of output load transients.

Cooling
AMIS5MP is specified for operation up to 10W output power. With an efficiency of 80% in case of large load current and not–cryogenic cooling, this translates in more than 2W lost in the converter (including the resistance of the inductor and of other

passive components). Most of this power is burnt by AMIS5 itself and needs to be transferred to the cooling system efficiently. The chosen qfn32 package has an exposed cooling pad to which the IC is directly attached, and the pad is soldered to the gnd plane of the AMIS5MP module. This plane is exposed as a large thermal pad in the bottom side, which must have a good thermal contact to the cooling system.

Module size, footprint, and stack height

The outline of the module, seen from above, is shown in the following image together with all relevant sizes. The 12-pin power connector is located to the left, while two 2.1mm diameter holes are located to the right giving the possibility to screw the module to a cooling plate to ensure efficient cooling. This is a temporary solution while a more compact and reliable arrangement is being studied. The highlighted rectangle in the middle of the module represents the shield, which is 8mm high, under which the ASIC, the main inductor and most of the other passives are arranged.
When mated, the connector height (from the motherboard to which the module is connected) is 5.97mm. Adding the 0.4mm thickness of the PCB and the 8.5mm height of the shield, the full stack height is just short of 15mm.



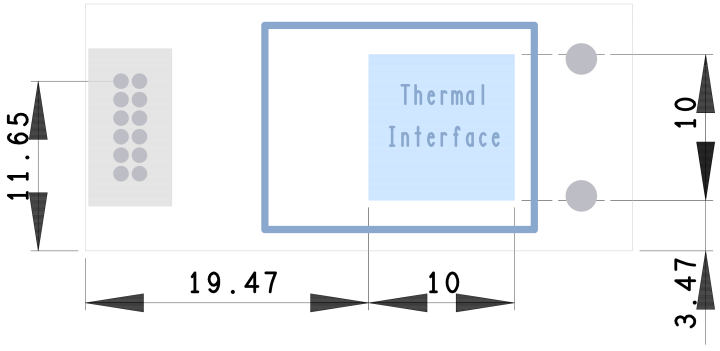
Top view of the AMIS5MP module with mechanical dimensions.

Power connector

The AMIS5MP module uses a 12-pin Samtec TFM-106-01-L-D male connector. The female mating connector is the SFM-106-01-L-D. All information about these connectors can be found in the Samtec web page (http://www.samtec.com/) under SFM or TFM, through hole, vertical, double row. In particular, at the time of releasing this document the footprint for the female connector could be found at http://www.samtec.com/documents/webfiles/cpdf/SFM-D-TH_Footprint.pdf, while the outline of the connector at http://www.samtec.com/documents/webfiles/cpdf/SFM-1XX-XX-XXX-D-XXX-MKT.pdf. To avoid difficulties in procuring small quantities of the female connector, samples can be provided with the AMIS5MP module on demand.

Thermal interface

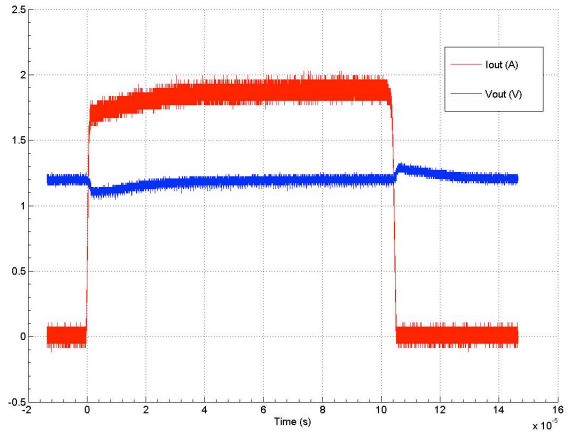
The bottom side of the module is equipped with a thermal interface of 10.62 mm x 11.81 mm in the form of exposed gnd plane. For the adequate operation of the module, this interface must be attached to a cooling element but electrically isolated from it. For this, an electrically insulating thermal pad must be inserted between the DCDC module and the receiving board (for instance the Bregquist Gap Pad 30S3000, Farnell code 878-3527). It must be noted that, when the module connector male is mated to the female on the user's board, there is a separation of 5.97mm between the thermal interface and the surface of the user's board. In this space, the user must accommodate the cooling plate. A complete mechanical solution for that purpose is under study and will be documented in another release of this document.



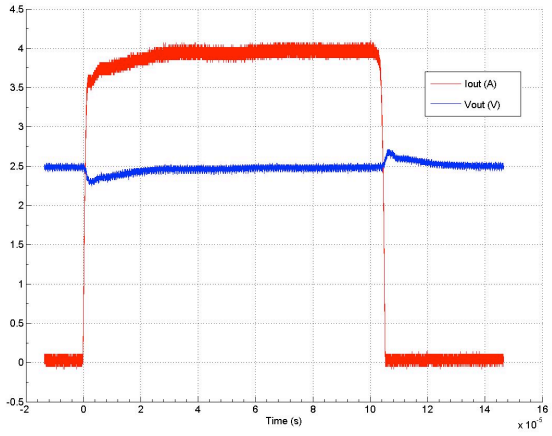
Top view of the module with size and position of the thermal interface

Typical operation waveforms

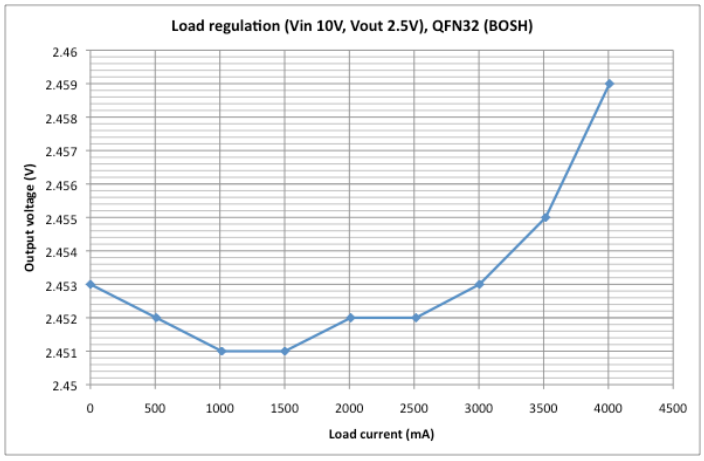
Since AMIS5MP is a prototype, the reported measurements have not been averaged over a number of modules but rather report typical performance.



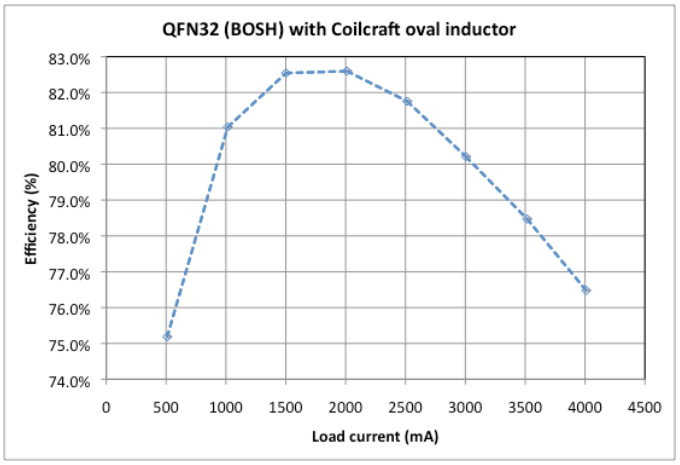
Transient load (0 to ~2A in ~800ns) at Vout=1.2V. Vin=10V



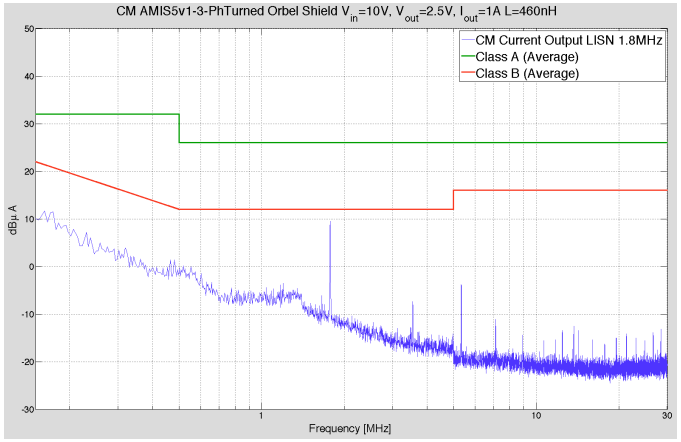
Transient load (0 to ~4A in ~800ns) at Vout=2.5V. Vin=10V

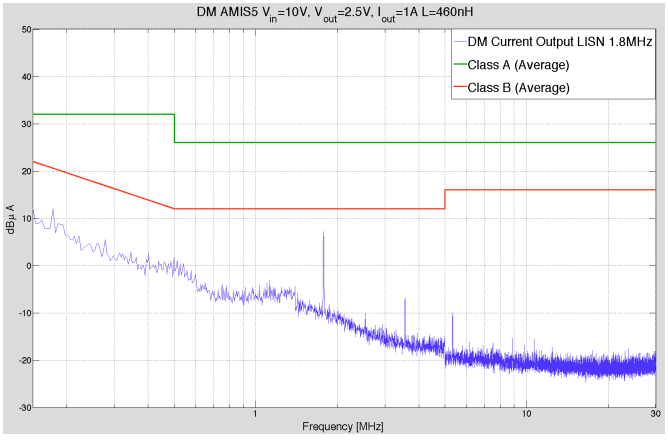


Load regulation performance for Vin=10V, Vout=2.5V, with the board in good thermal contact with a cooling pad at 18°C.



Converter efficiency measured for Vin=10V, Vout=2.5V, with the board in good thermal contact with a cooling pad at 18°C.





Output common mode (left) and differential mode (right) currents of the typical AMIS5MP module at Vin=10V, Vout=2.5V, Iout=1A. Noise is kept below the Class B limit of the CISPR11 reference standard, with only the fundamental at the switching frequency exceeding 0 dBµA. These noise properties are obtained with the shield mounted on the converter. In this configuration, the residual electric field radiated by the converter is not measurable with the equipment available.

Revision history

Revision	Date	Description
1.0	May2013	First release of the document
1.1	June2013	Addition of the height of the full stack (mating connector, PCB, shield)
1.2	July2013	Correction of Pin assignment numbers (it was correct on plan, but wrong on table)
1.3	Nov2013	Addition of size in the image of the top view of the module