AMIS2

Data sheet
10/12/2008
S. Michelis

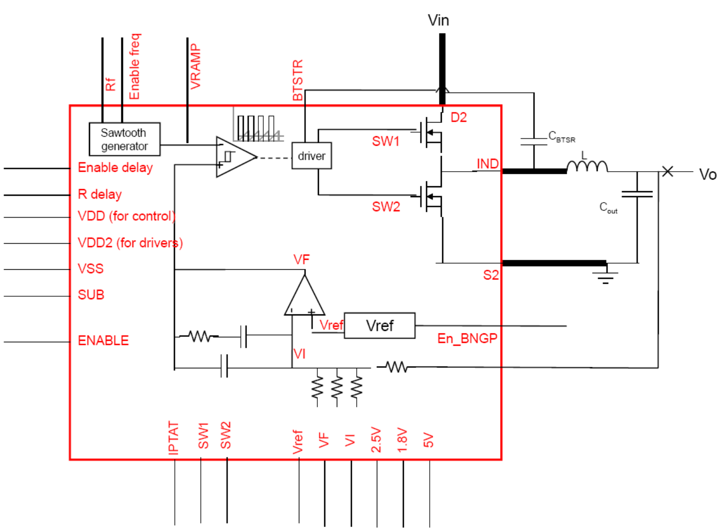
Single-Phase Buck DC/DC converter

AMIS2 is a single-phase voltage-mode PWM controller with integrated synchronous rectified MOSFET.
The output voltage of the converter can be precisely regulated with an external reference voltage (nominally 1.2V).
The external oscillator is adjustable from 250kHz to 3MHz.

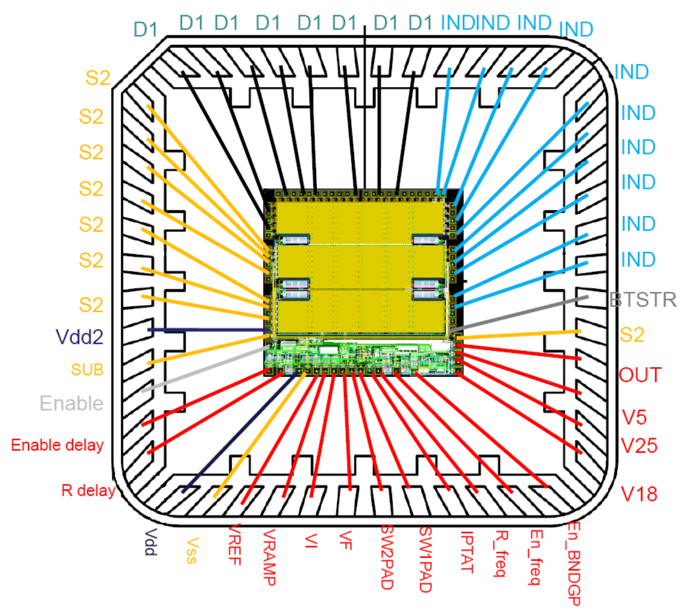
Features

VIN and Power Rail Operation from +3.3V to +12V
Fast Transient Response - 0 to 100% Duty Cycle
14MHz Bandwidth Error Amplifier with 10V/μs Slew Rate
Internal oscillator fixed at 1Mhz, programmable from 400kHz to
3MHz with external resistor
Internal voltage reference (nominally (1.2V)
Remote Voltage Sensing with Unity Gain
Programmable delay between gate signals
Integrated feedback loop with bandwidth of 20Khz

Block Diagram



Pinout



Absolute Maximum Ratings Thermal Information

Input Voltage, D1. . . . . 0V to +12.0V
BTSTR Voltage, VBTSTR . . . . 0 to +15.63V
BOOT To IND Voltage (VBOOT-VPHASE). . . . . . 0 V to 3. 3V
IND Voltage, VIND . . . . 0V to +12.0V
S2 Voltage (power ground) ……………………….. 0V
VDD Voltage, VDD…………………………………….0V to 3.63V
VDD2 Voltage, VDD2…………………………………0V to 3.63V
VSS Voltage, VSS……………………………………..0V to 3.63V
VREF Voltage, VREF…………………………………0V to 3.63V
VI Voltage, VI…………………………………………..0V to 3.63V
VF Voltage, VF………………………………………...0V to 3.63V
VRAMP Peak Voltage, VRAMP……………………..0V to 3.63V
SUB substrate voltage, VSUB ………………………0V
Enable delay, En_delay………;;;…………………..0V to 3.63V
Res delay, R_delay………;;;;……………………….0V to 3.63V
Enable frequency, En_freq.;;….;……………………..0V to 3.63V
Res frequency, R_freq…………………………………0V to 3.63V
Enable bandgap, En_BNGP…………………………..0V to 3.63V
Out, OUT………………………………………………...0V to 6V
5V enable, V5 …………………………………………..0V to 3.63V
2.5V disable, V25 ………………………………..……..0V to 3.63V
1.8V enable, V18 ……………………………………......0V to 3.63V
Temperature control, IPTAT ……………………….....0V to 3.63V
SW1 gate control, SW1PAD..……………………….....0V to 3.63V
SW2 gate control, SW2PAD..……………………….....0V to 3.63V

Recommended Operating Conditions

Input Voltage, D1. . . . . 3.3V to 12V ±10%
BOOT To IND Voltage (VBOOT-VPHASE). 3.3V
S2 Voltage (power ground) ………………………………… 0V
VDD Voltage, VDD…………………………………………….3.3V
VDD2 Voltage, VDD2………………………………………….3.3V
VSS Voltage, VSS……………………………………………….0V
VREF Voltage, VREF…………………………………………1.2V
VRAMP Peak Voltage, VRAMP……………………………..3.3V
SUB substrate voltage, VSUB ………………..………………0V
Enable delay, En_delay………;;;…………………..0V to 3.3V
Res delay, R_delay………;;;;……………………….0V to 3.3V
Enable frequency, En_freq.;;….;……………………..0V to 3.3V
Res frequency, R_freq…………………………………0V to 3.3V
Enable bandgap, En_BNGP…………………………..0V to 3.3V
Out, OUT………………………………………………...0V to 6V
5V enable, V5 …………………………………………..0V to 3.3V
2.5V disable, V25 ………………………………..……..0V to 3.3V
1.8V enable, V18 ……………………………………......0V to 3.3V
Temperature control, IPTAT ……………………….....0V to 3.3V
SW1 gate control, SW1PAD..……………………….....0V to 3.3V
SW2 gate control, SW2PAD..……………………….....0V to 3.3V

Electrical Specifications ***Recommended Operating Conditions, Unless Otherwise Noted***

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE						
VREF	Input Reference Voltage			1.2		V
VD1	Input Voltage		3.3		22	V
VDD	Input logic part voltage		3	3.3	3.63	V
VDD2	Driver voltage		3	3.3	3.63	V
VSS	Ground logic part voltage			0		V
VSUB	Substrate voltage			0		V
VS2	Ground power part voltage			0		V
VGND_D	Ground voltage for diode			0		V
ID1	Maximum power input current				4	A
OSCILLATOR						
OSCFMAX	Nominal Maximum Frequency		-	3000	-	kHz
OSCFMIN	Nominal Minimum Frequency		-	250	-	kHz
OSCFNOM	Nominal frequency		-	1000	-	kHz
ΔVOSC	Ramp Amplitude		-	3.3	-	VP-P
VOSC_MIN	Ramp Bottom		-	3.3	-	V
PWM						
DMAX	Maximum Duty Cycle		-	100	-	%
DMIN	Minimum Duty Cycle		-	0	-	%
ERROR AMPLIFIER						
	DC Gain	CL = 1p at VF Pin	-	87	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1p at VF Pin	-	14	-	MHz
SR	Slew Rate	CL = 1p at VF Pin	-	10	-	V/µs
ERROR AMPLIFIER						
	DC Gain	CL = 1p at VF Pin	-	87	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1p at VF Pin	-	14	-	MHz
SR	Slew Rate	CL = 1p at VF Pin	-	10	-	V/µs

Functional Pin Description

D1 (Power Input)

This pin should be tied to the input rail with a capacitor of 20uF between D1 and S2 to prevent noise injection into the generator. It provides power to the power part of the circuit.

S2 (Power ground)

This pin should be tied to the ground of the power part.

VDD (Analog Circuit Bias)

This pin provides power for the AMIS2 analog circuitry. The pin should be connected to a 3.3V bias through an RC filter to prevent noise injection into the analog circuitry.

VDD2 (Driving Circuit Bias)

This pin provides power for the AMIS2 driving circuitry. The pin should be connected to a 3.3V bias through an RC filter to prevent noise injection into the analog circuitry.

VSS (Analog Ground)

Signal ground for the IC. All voltage levels are measured with respect to this pin. This pin should not be left floating.

SUB (substrate potential)

This pin is the substrate contact for the IC. This should be connected to ground.

Enable (Circuit enabler)

This pin is the enabler of the circuit. If it is connected to Vdd the circuit is enabled, otherwise if it connected to Vss it is disabled.

VRAMP (Sawtooth waveform input)

this pin is used for monitoring the sawtooth waveform.

IND (Inductor voltage)

This pin connects to the source of the high side MOSFET and the drain of the low side MOSFET. This pin represents the return path for the high side gate driver.

BTSTR (Bootstrap voltage)

This pin provides the bootstrap bias for the high side driver. The absolute maximum voltage differential between BTSTR and IND is 3.3V (including the voltage added due to the overcharging of the bootstrap capacitor); its operational voltage range is 3V to 3.63V with respect to IND.

VF (Output of the error amplifier)

This pin is the error amplifier output. It can be connected to the VI pin through the desired compensation network. In parallel with the embedded one.

VI (Inverting input of the error amplifier)

This pin provides remote sense for the AMIS2. This pin is the inverting input of the error amplifier. The voltage at this pin should be set equal to the internal system reference voltage (1.2V typical). This is done through the internal resistor. For default the resistor that allow to generate the 2.5 V is connected to Vss. This pin should can be connected to VOUT with an additional compensation network.

VREF (Non-inverting input of the error amplifier)

This pin monitors the voltage reference for the AMIS2. This pin is the non-inverting input of the error amplifier. It should be left floating.

En_delay (Enable delay)

This pin enables the possibility to change the delay between the gate signal of the two power transistor. Nominally this delay is 50ns and in this case the pin has to be left floating. In order to change the delay the pin has to be connected to Vss and it is mandatory to connect a resistor to R_delay pin.

R_delay (Res delay)

This pin allows connecting a resistor to change the delay between the gate signal of the two power transistor

En_freq (Enable frequency)

This pin enables the possibility to change the frequency of the sawtooth signal. Nominally this frequency is 1Mhz and in this case the pin has to be left floating. In order to change the frequency the pin has to be connected to Vss and it is mandatory to connect a resistor to R_freq pin.

R_freq (Res frequency)

This pin allows connecting a resistor to change the frequency of the sawtooth signal.

En_BNGP (Enable bandgap)

This pin allows enabling the trimming on the bandgap generator. It should be left floating.

OUT (Out)

This pin has to be connected to the output voltage

V5 (5V enable)

If this pin and the V25 pin are connected to Vss, AMIS2 is set to provide 5V at the output

V25 (2.5V disable)

If this pin is left floating, AMIS2 is set to provide 2.5V at the output. If it is connected to Vss AMIS2 is set to provide 1.2V at the output

V18 (1.8V enable)

If this pin and the V25 pin are connected to Vss, AMIS2 is set to provide 1.8V at the output

IPTAT (Temperature control)

This pin allows monitoring the temperature of the chip.

SW1PAD (SW1 gate control)

This pin allows monitoring the gate signal of the high side power transistor.

SW2PAD (SW2 gate control)

This pin allows monitoring the gate signal of the low side power transistor.

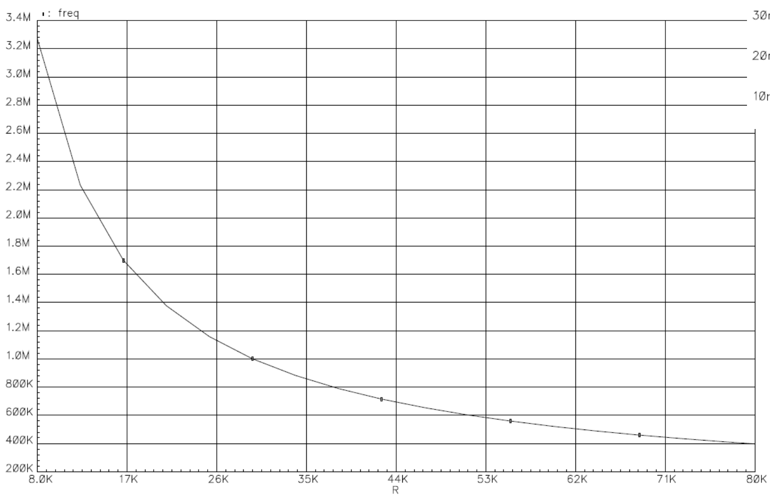
Functional Description

Initialization

The AMIS2 doesn't automatically initialize upon receipt of power. It requires special sequencing of the input supplies. The Power supply for the power part should be switched on for first.

Oscillator/VRAMP, En_freq, R_freq

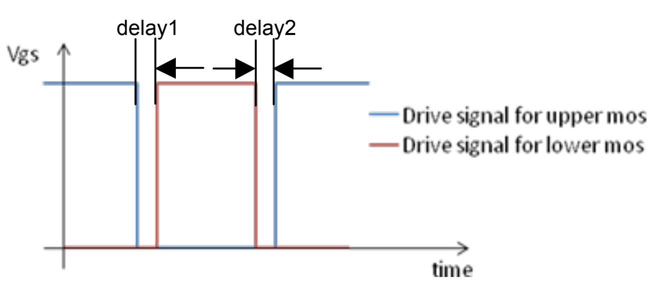
The internal oscillator provides by default a sawtooth signal with a frequency of 1Mhz. has to be connected to a sawtooth waveform generator, provided for PWM modulation. The bottom of the oscillator waveform is set at 0V. The ramp's peak to peak amplitude is 3.3V. The frequency of the waveform can be decided between 400Khz and 3MHz setting the resistance connected between Vss and R_freq pin and connecting En_freq to Vss. The value of the resistor can be chosen looking at the following table.



Leaving floating R_freq and En_freq the frequency is automatically set at 1Mhz.

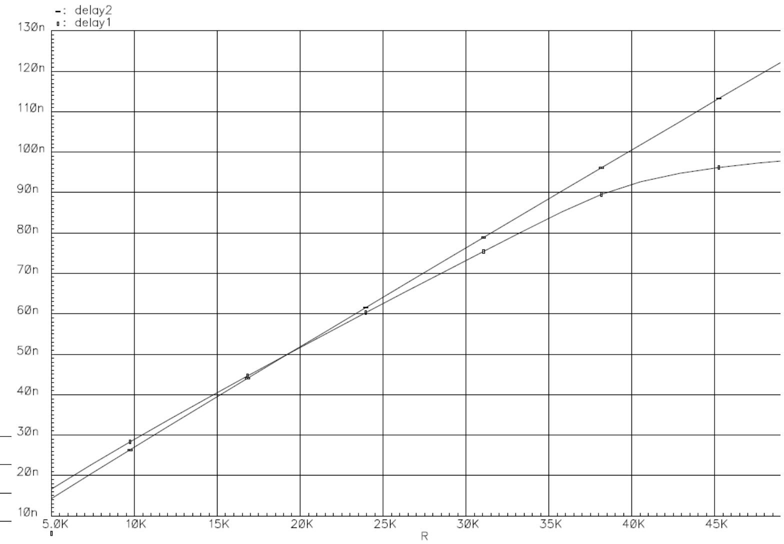
Delay between power transistor gate signal/En_delay and R_delay

It is necessary to avoid any overlap of the two gate control signals to prevent shoot-through between the input node and ground at every cycle which could damage or at least drastically affect the efficiency of the converter. The correct timing of the two gate signals is depicted in the following figure.



Leaving the pins En_delay and R_delay floating delay1 and delay2 are set at 55ns.

Connecting En_delay to Vss the delays can be modified setting the resistor connected between Vss and R_delay pin. The following table gives the values of the desired delays value versus the resistance.



Output voltage regulation/OUT, V5, V25, V18

The output voltage can be regulated setting properly the pin.
The OUT pin has to be always connected to the output node.
In order to obtain an output voltage of:

- 2.5V the pins V5, V25 and V18 need to be left floating
- 5V the pins V25 and V5 have to be connected to Vss, while V18 pin needs to be left floating
- 1.8V the pins V25 and V18 have to be connected to Vss, while V5 pin needs to be left floating
- 1.2V the pin V25 has to be connected to Vss, while V18 and V5 need to be left floating

Application Guidelines

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device over-voltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET is carrying the output inductor current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.
The power train components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, CIN, especially the high frequency decoupling, and the power

switches. The design of AMIS2 is already made in order to facilitate the placement of CIN between D1 and S2.
Locate the output inductor and output capacitors between AMIS2 and the load. Locate all the high-frequency decoupling capacitors (ceramics) as close as practicable to their decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND immediately next, or even onto the capacitor's grounded solder pad and using several of them in order to reduce the inductance.
The critical small signal components include the bypass capacitors for VDD. Locate the bypass capacitors close to the device. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. Place all the other highlighted components close to the respective pins of the AMIS2.
A multi-layer printed circuit board is recommended. The figure 1 shows the connections of the critical components of the converter.

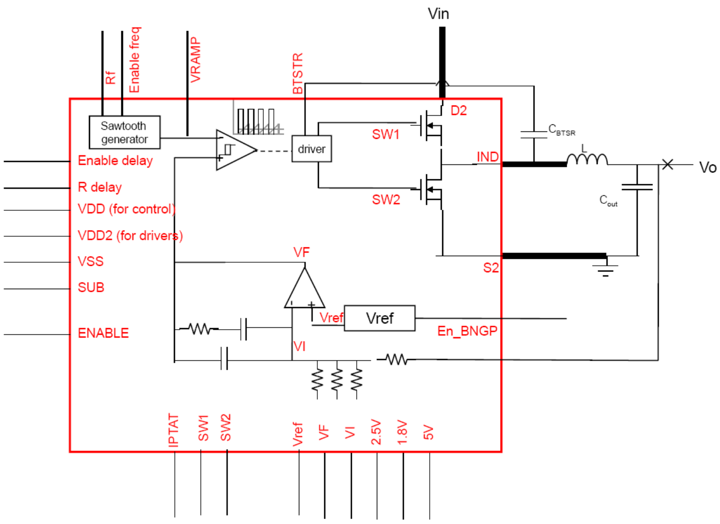


Fig. 1 connections of the critical components of the converter

Note that capacitors CIN and COUT could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, to a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the IND island as small as practicable. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for large current-carrying circuit nodes. Use the remaining printed circuit layers for small signal wiring.
Size the trace interconnects commensurate with the signals they are carrying. Use narrow and short traces for the high-impedance, small-signal connections, such as the feedback, compensation, sawtooth set and reference input.

Component Selection Guidelines

Output Inductor Selection

The very high external magnetic flux density (up to 4 T) strongly limits the choice of the inductor because it prevents the possibility to use magnetic cores. This is due to the saturation of all ferromagnetic materials. Ferromagnetic materials as permendur and iron can reach values of saturation flux density around 2 T but at 4 T all the magnetic domains align their dominant magnetic orientation in the direction of the applied magnetic field. In this case the core can make no further contribution to flux growth and any increase thereafter is limited to that provided by the air permeability. Therefore, it is necessary to use an air core inductor in order to avoid any problem of magnetic saturation of the core and obtain an inductor whose value does not depend on the external magnetic field. Without a high permeability core it is necessary to have higher length to achieve a given inductance value, increasing in a substantial way the volume. More turns means larger coils, lower self-resonance and higher copper loss. The air core inductors produce a reduction of the efficiency of the system due to its parasitic resistance in comparison to an inductor with a ferromagnetic core. Air core inductors with an inductance value between 500nH and 1μH are foreseen as a good trade-off.
The inductor value determines the converter's ripple current . Its peak to peak value is approximated by the following equation:

$$I_{PP} = D\frac{Vin - Vout}{L}T$$

where D is the PWM duty cycle and T the period of the PWM modulation.
Increasing the value of inductance reduces the ripple current. However, the large inductance values reduce the converter's response time to a load transient.
One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the AMIS2 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.
High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements.
High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.
Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading and can increase

the ripple of the output load. The simplified formula in order to calculate the output ripple is the following:

$$V_{PP} = I_{PP}\left(\frac{1}{8C_{out}}T + ESCR + \frac{1}{DT}ESCL\right)$$

where I_{PP} is the value calculated for the inductor current, Cout is the output capacitor, ESCR and ESCL are respectively the equivalent series resistance and inductance of Cout.
ESCL is a parameter that is difficult to know but it can strongly affect the value of the output ripple. Even the via connection to ground can introduce extra series inductance, therefore it is suggested to increase the number of vias to reduce this effect.
A typical value of output capacitor is 20uF that seems to be a good balance between ESCR and ESCL at the operating frequency of 1-3 Mhz.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOS turns on. Place the small ceramic capacitors physically between the drain D1 and the source S2.
The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximated in the following equation:

$$I_{IN,RMS} = I_{out}\sqrt{D}\sqrt{1+\frac{1}{12}\left(\frac{Vin-Vout}{LI_{out}}DT\right)^2}$$

The input capacitor will act as an LC filter considering the inductance of the power supply cables. This LC filter introduce a transfer function that can modify the stability of the controller. Please contact stefano.michelis@cern.ch for better information on input capacitor.
A typical value for input capacitor is 20uF.

References

[1] S. Michelis, F. Faccio, P. Jarron, M. Kayal, *Air core inductors study for DC/DC power supply in harsh radiation environment,* NEWCAS-TAISA conference 2008

[2] S. Michelis, F. Faccio, A. Marchioro, M. Kayal, *Inductor based switching DC-DC converter for low voltage power distribution in SLHC*, TWEPP 2007, Prague

[3] S. Maniktala, *Switching power supplies A to Z* , ed. Newnes, 2006, Burlington, USA.

[4] R. Redl. “DC-DC converters, topologies and control techniques. Converter modeling and feedback loop design”, *EPFL-MEAD power management course*, 3-7 September 2007, Lausanne, Switzerland.

[5] N. Femia., “Control switching techniques for switching power supply, ” *power design technical course 2007*, National semiconductor, 2007 Zurich, Switzerland.

[6] W.H. Lei, T.K. Man, “A general approach for optimizing dynamic response for buck converter, *On semiconductor*, application note, AND8143/D, April 2004-Rev.0